

Jedi 15"/17" Schematics

WhiskyLake - U/2GB VRAM

2019-01-03

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>		
DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Cover Page		
Size A3	Document Number Jedi15"/17" WHL-U	Rev A00
Date: Tuesday, January 08, 2019	Sheet 1	of 106

Project code: 4PD0GE010001
PCB P/N: 18718
Revision: X02



Main Func = CPU

- 24 PECL_CPU
- 24,44,46 PROCHOT#_CPU
- 55 TOUCH_PANEL_INTRA
- 24,65 TP_WAKE_KBC#
- 55 TOUCH_PANEL_PD#
- 17 H_CUPUPWRGD

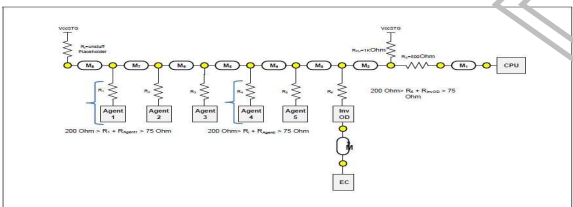
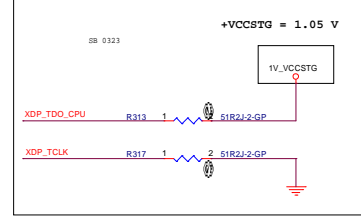
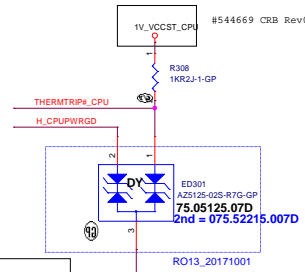
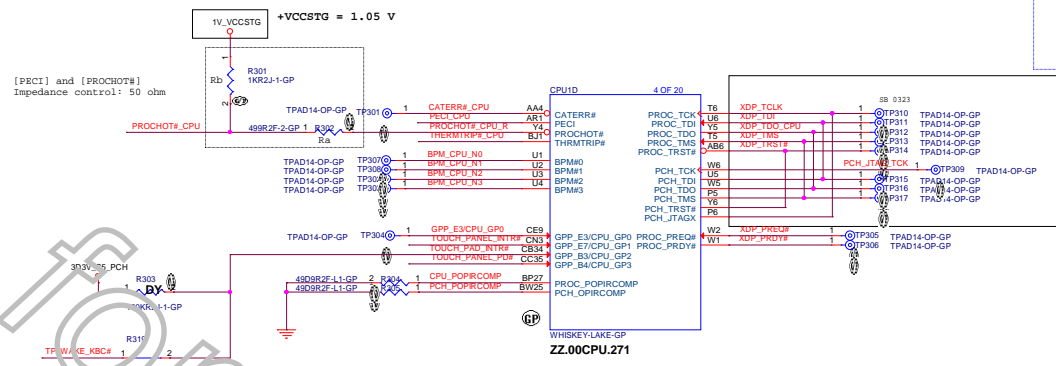
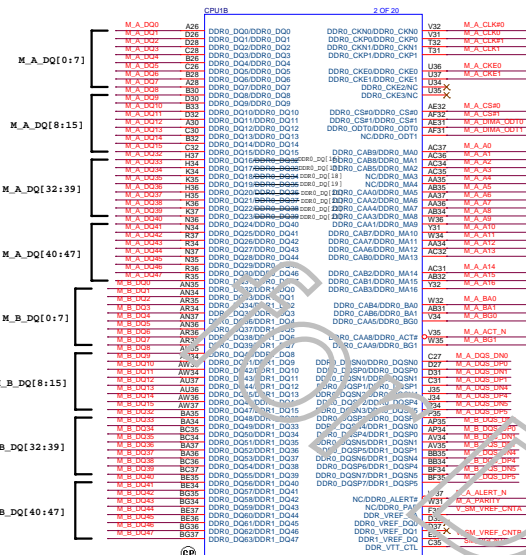
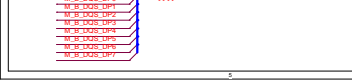
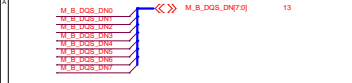
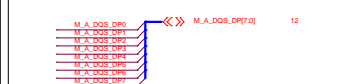
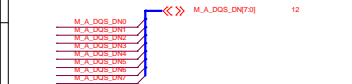
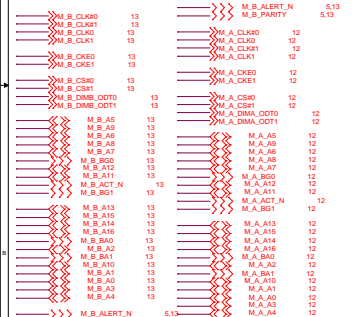
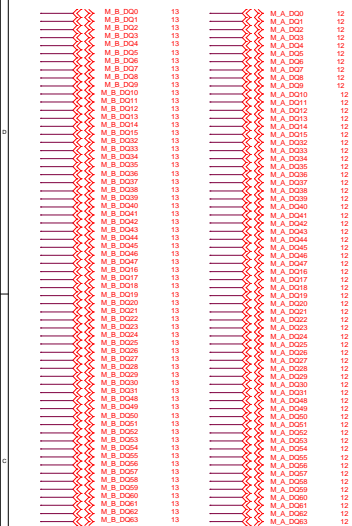


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values		Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinod=75-200Ω					
Platform resistors tolerances		± 5%					



DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed, also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

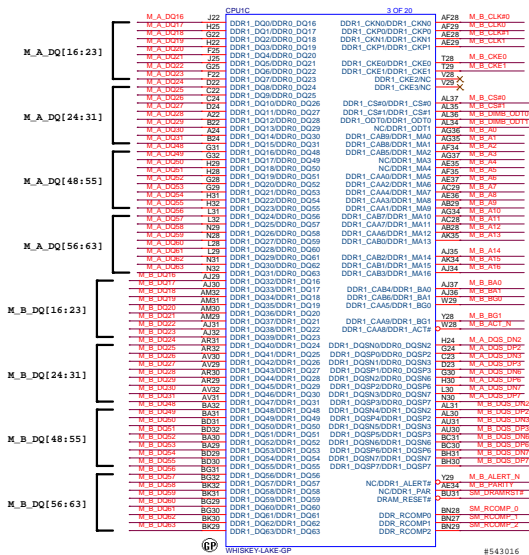
4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
	DDR4 SODIMM	DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
	DIMMs	DIMMs	ODT[1:0]	

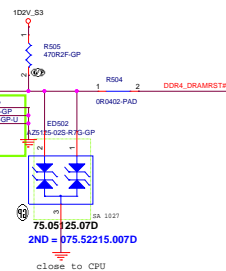
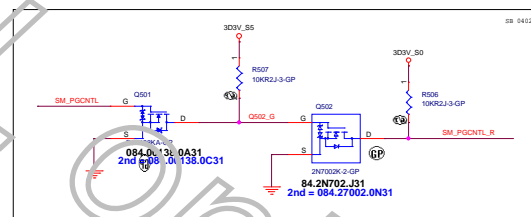
Note:

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.



Design Guideline:
SM_RCMP keep routing length less than 500 mils.

Layout Note:

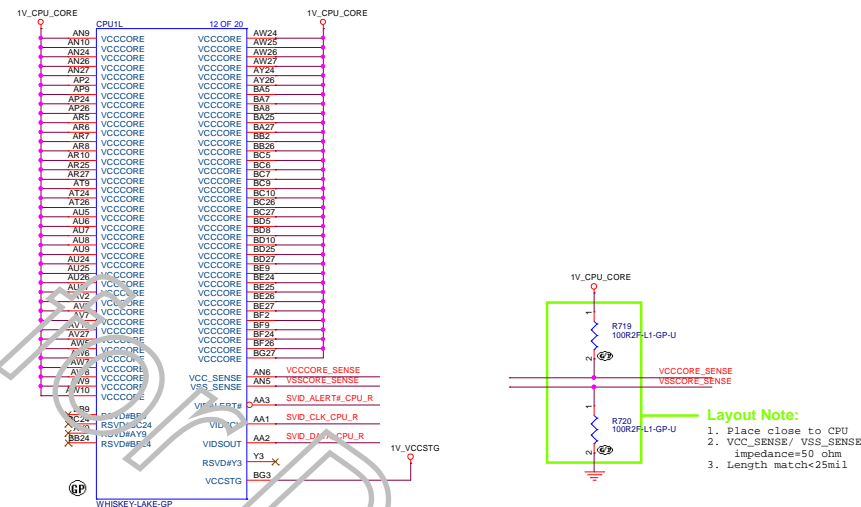


Jed LMA/CH 2011



46 VCCCORE_SENSE<<<====
46 VSSCORE_SENSE<<<====

46 VIDSOUT_CPU_R<<<====
46 VIDSCK_CPU_R<<<====
46 PWR_VCORE_ALERT#<<<====



Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543010:

SVID DATA

SVID CLOCK

SVID ALERT

Figure 7-19. Routing Illustration for SVID Topology

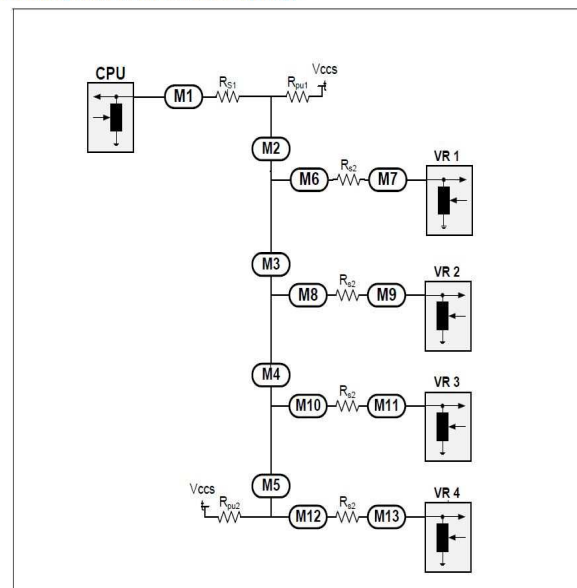


Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11

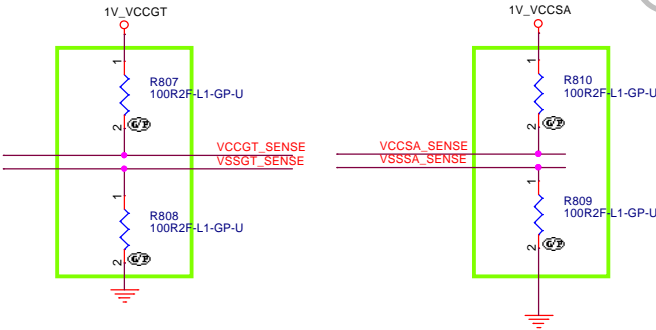
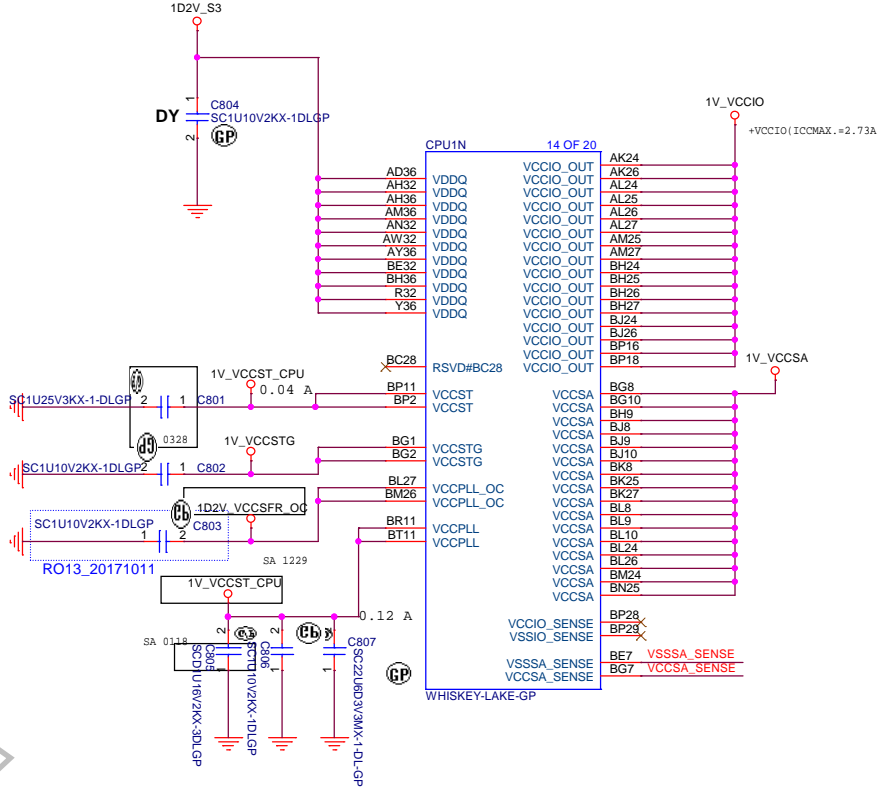
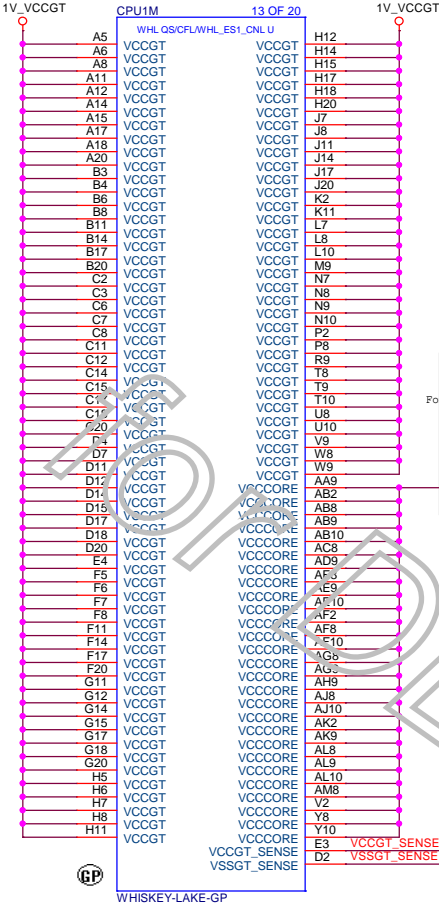
Topology Guidelines	
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

Jedi UMA/DS 2N1

Main Func = CPU

46	VSSSA_SENSE	<<<<	_____
46	VCCSA_SENSE	<<<<	_____
46	VCCGT_SENSE	<<<	_____
46	VSSGT_SENSE	<<<	_____

Pin Number	CFL-U43E	WHL E51 Netname	WHL E52 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



Layout Placement Request

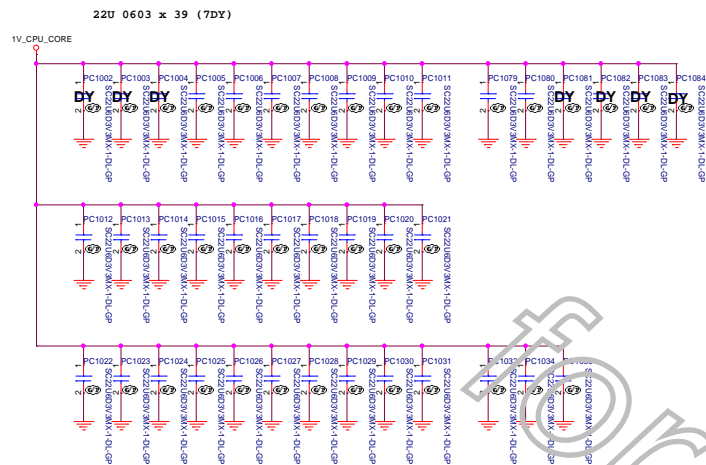
for DELL only

(Blanking)

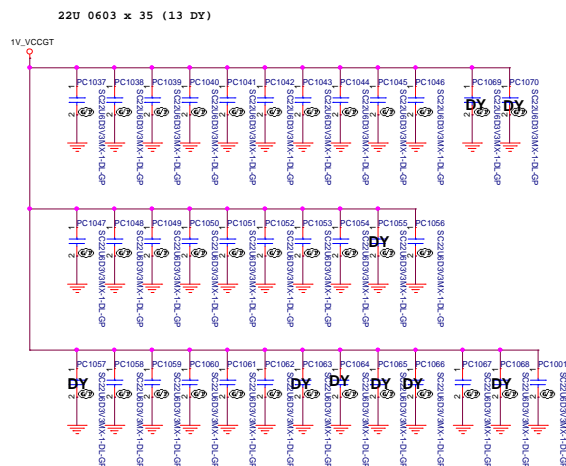
Jedi UMA/DIS 2IN1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (RSVD)			
Size A3	Document Number Jedi15"/17" WHL-U		Rev A00
Date: Tuesday, January 08, 2019		Sheet 9	of 106

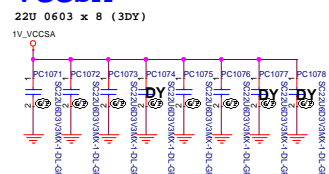
1V_CPU_CORE



VCCGT



VCCSA



11.3.1 Whiskey Lake U 4+2 Decoupling Requirement

Table 11-1. Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
VCCORE Power Plane at VR output	4x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output

Notes:

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
		8x 10uF 0402	
VCCGT		18x 47uF 0805 (6.3V)	Place as close to the package as possible. Can be placed on as either Primary or back side cap.
	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

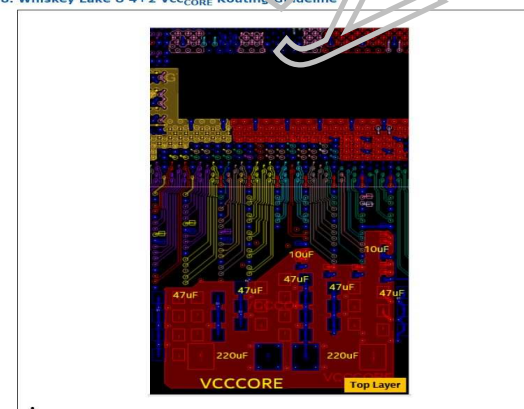
Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCSA		4x 0402	Placeholder only.
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		
VDDQ		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
VCCIO	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
VCCPLL_OC	4x 0402		Placeholder Only
	1x 1uF 0402		Do not merge VCCPLL, VCCPLL_OC and VCCGT to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VCCPLL	1x 0.1uF 0201		Place as close as possible to BGA.
		1x 1uF 0402	Place as close as possible to BGA and can be placed on as either Primary or backside cap.
		1x 0805	Placeholder Only. Can be placed on as either Primary or back side cap.
VCCGT	1x 1uF 0402		
VCCSTG	1x 1uF 0402		

Notes:

- The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
- Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source

Figure 11-8. Whiskey Lake U 4+2 VCCORE Routing Guideline



<Core Design>

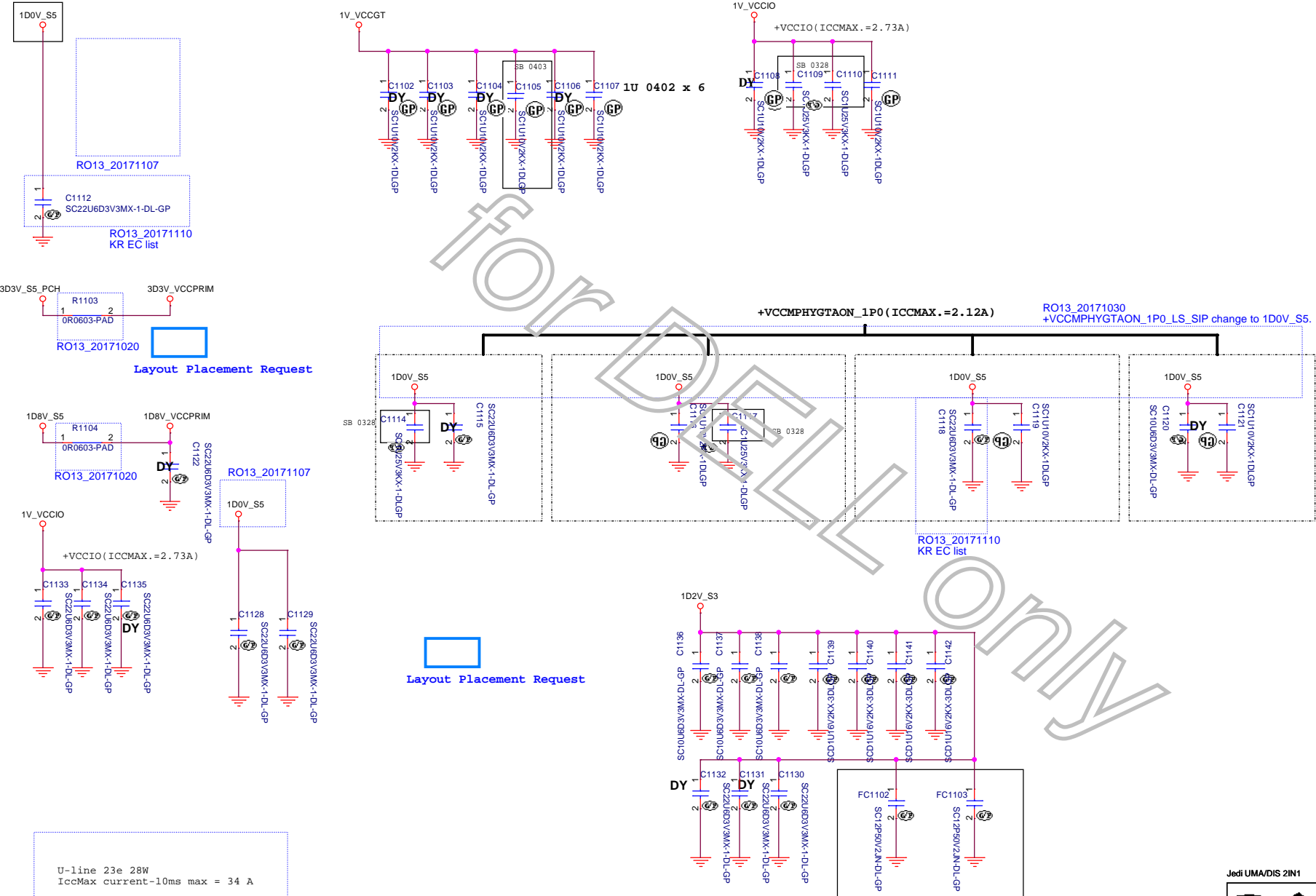


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU (Power CAP1)
Size			Jedi15/17" WHL-U
Date			Tuesday, January 09, 2019
Rev			A00
Sheet			10 of 109

Main Func = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



Layout Note:

1uF:

- C1174 near N15
- C1180 near K15
- C1173 near AF20
- C1172 near N18
- C1175 near AB19

22uF :


- C1182 C1184 near N15

10uF:

- C1176 near N15

U-line 23e 28W
IccMax current-10ms max = 34 A

RF request 2018/09/28 modify



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (Power Cap2)

Size A3

Document Number

Jedi15"/17" WHL-U

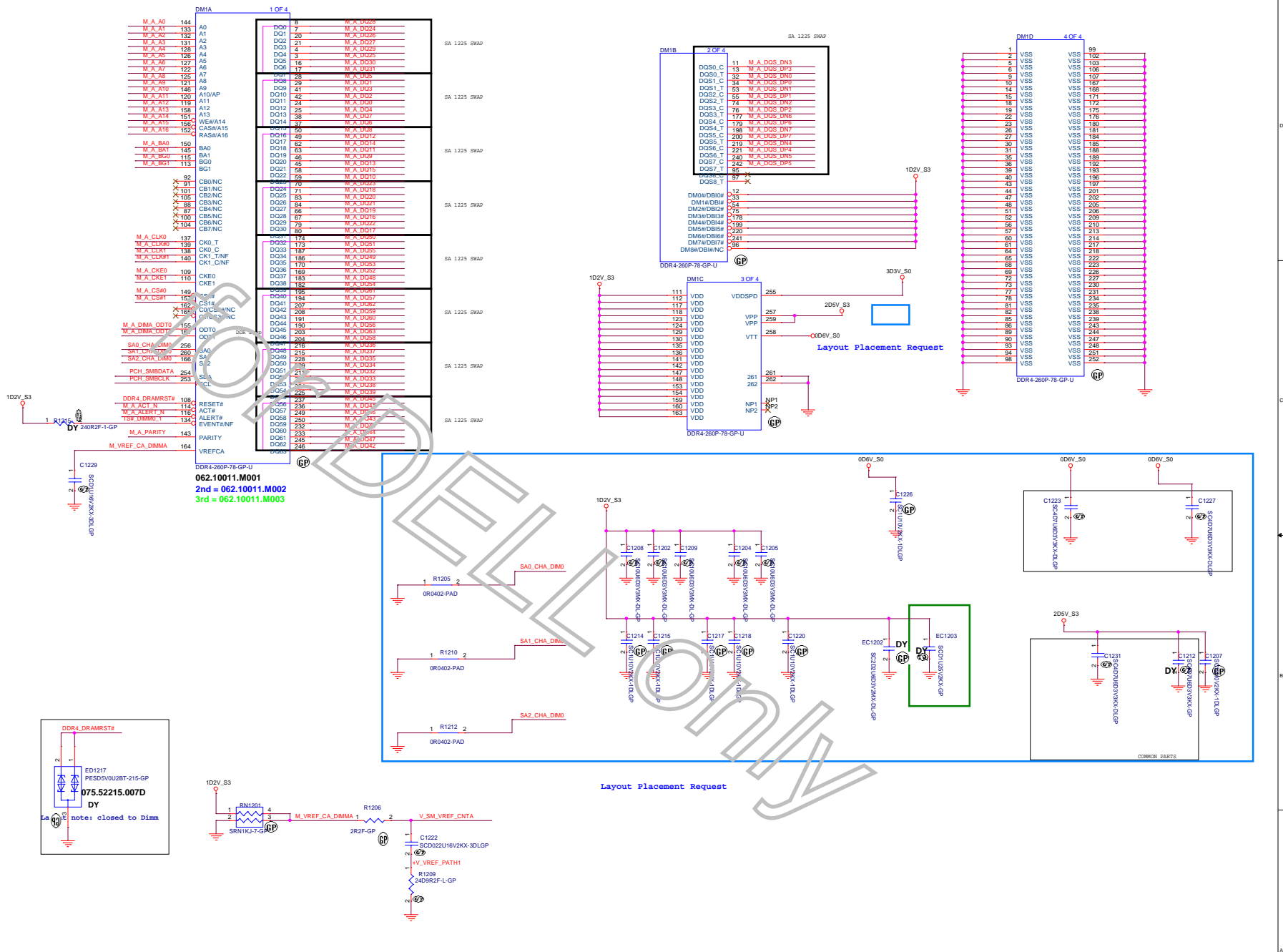
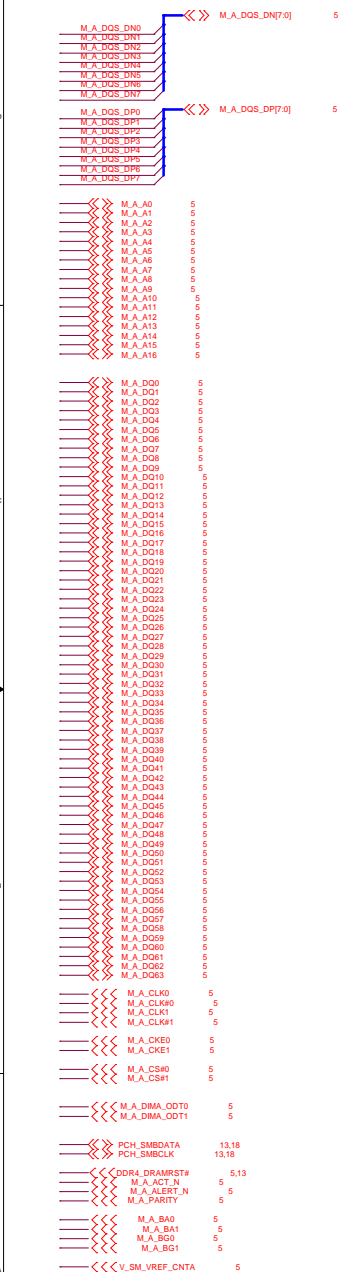
Rev

A00

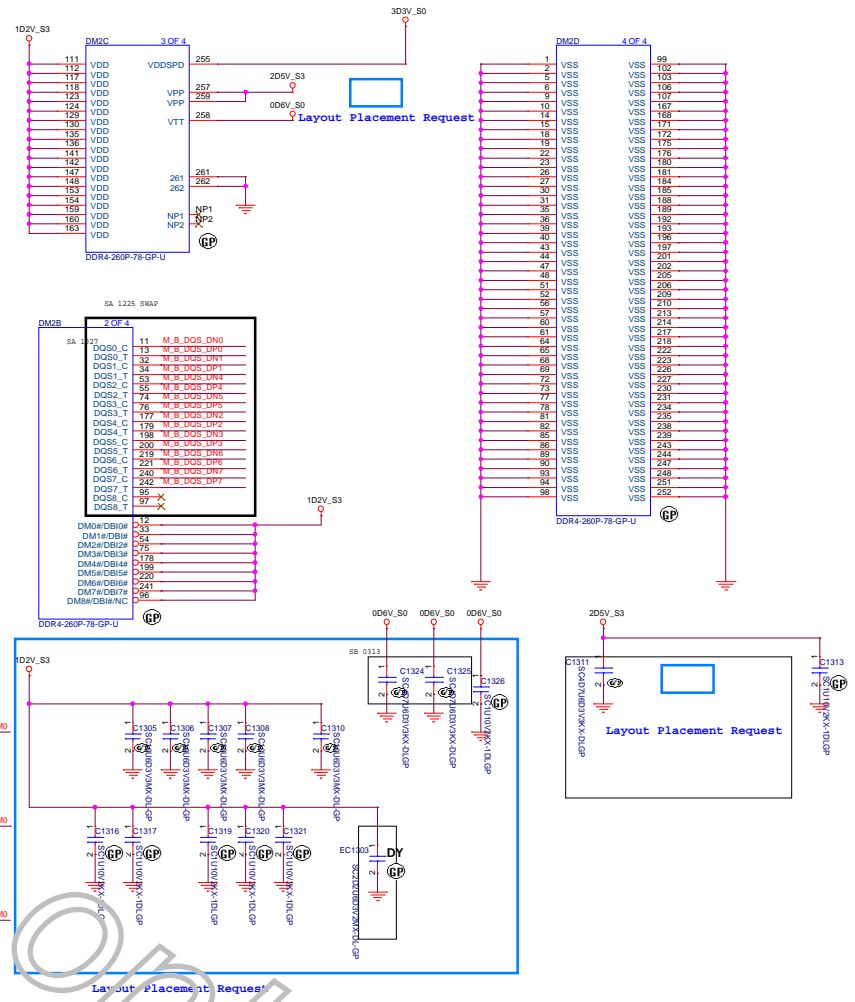
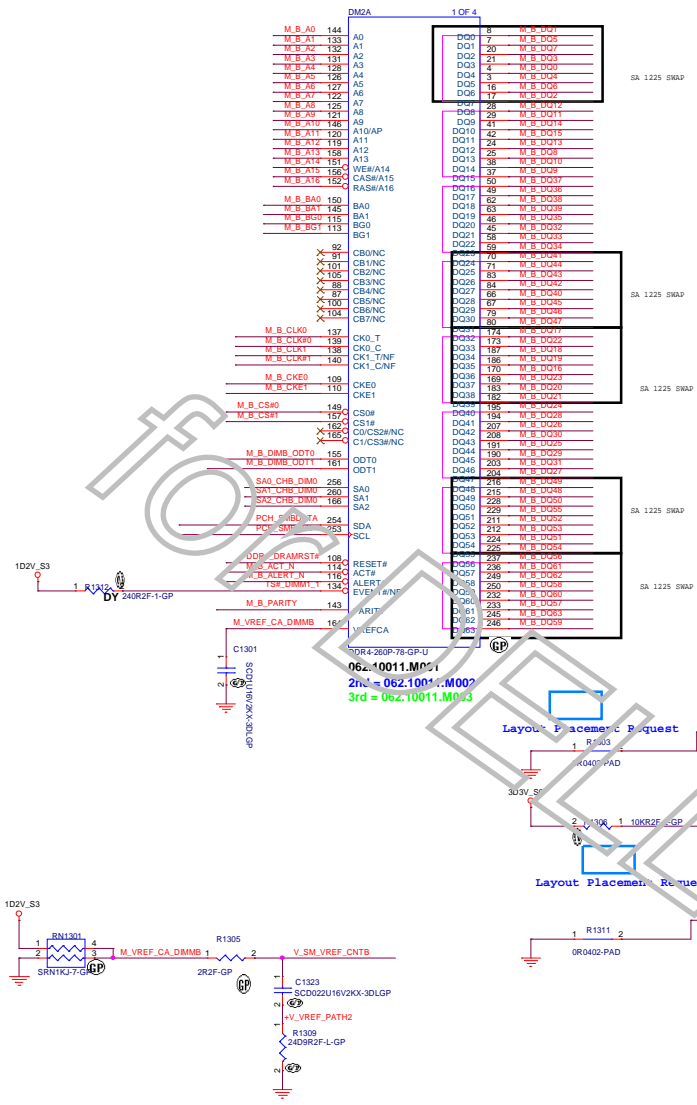
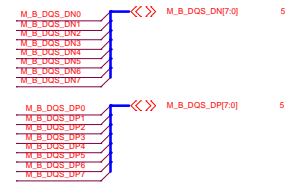
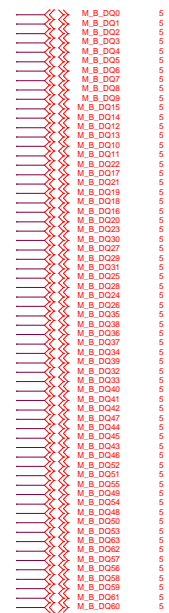
Date: Tuesday, January 08, 2019

Sheet 11 of 106

Main Func = MEMORY




=====	M_B, A0	5
=====	M_B, A1	5
=====	M_B, A2	5
=====	M_B, A3	5
=====	M_B, A4	5
=====	M_B, A5	5
=====	M_B, A6	5
=====	M_B, A7	5
=====	M_B, A8	5
=====	M_B, A9	5
=====	M_B, A10	5
=====	M_B, A11	5
=====	M_B, A12	5
=====	M_B, A13	5
=====	M_B, A14	5
=====	M_B, A15	5
=====	M_B, A16	5
=====	M_B, BAO	5
=====	M_B, BA1	5
=====	M_B, BBO	5
=====	M_B, B01	5
=====	M_B, C00	5
=====	M_B, C040	5
=====	M_B, CLK1	5
=====	M_B, CLK61	5
=====	M_B, CK02	5
=====	M_B, CK01	5
=====	M_B, CS00	5
=====	M_B, CS01	5
=====	M_B, DMB, 0070	5
=====	M_B, DMB, 0071	5
=====	PCH_SMBDATA	5
=====	PCH_SMBCLK	5
=====	DDR4_DRAMRST#	5
=====	M_B, ACT_N	5
=====	M_B, ALERT_N	5
=====	M_B, PARITY	5
=====	V_S1_VREF_CNTB	5



for DELL only

(Blanking)

Jedi UMA/DIS 2IN1

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title DDR (RSVD) (DDR4-CHA1)					
Size A4		Document Number Jedi15"/17" WHL-U			Rev A00
Date: Tuesday, January 08, 2019		Sheet 14		of 106	

Main Func = PCH

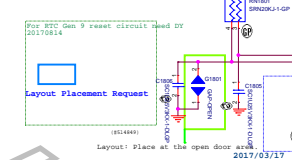
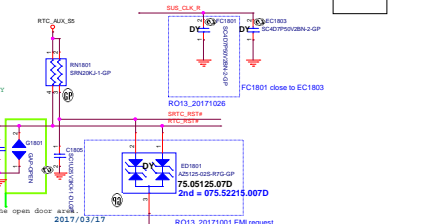
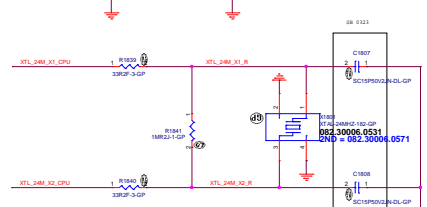
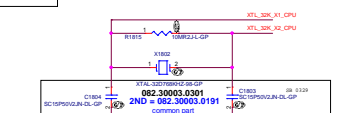
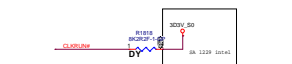
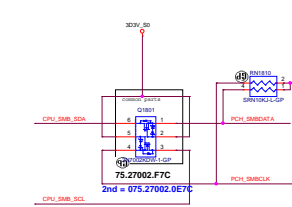
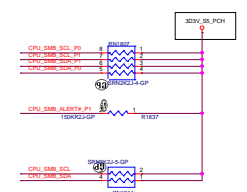
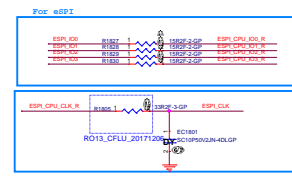
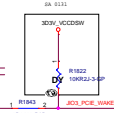
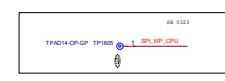
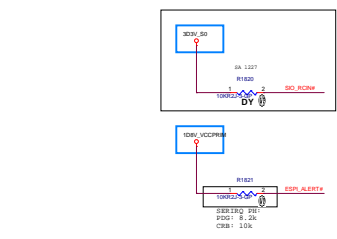
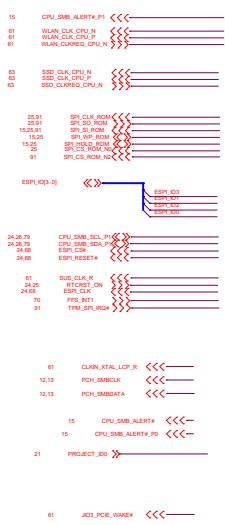


Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

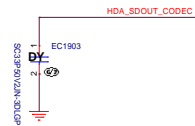
eSPI Enable Strap (eSPI_EN) Value	Boot BIOS Strap (BIOS) Value	EC Connection	Boot (BIOS) Flash Connection
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	LPC

Table 9-1: Functions Strap Definitions (Sheet 2 of 3)

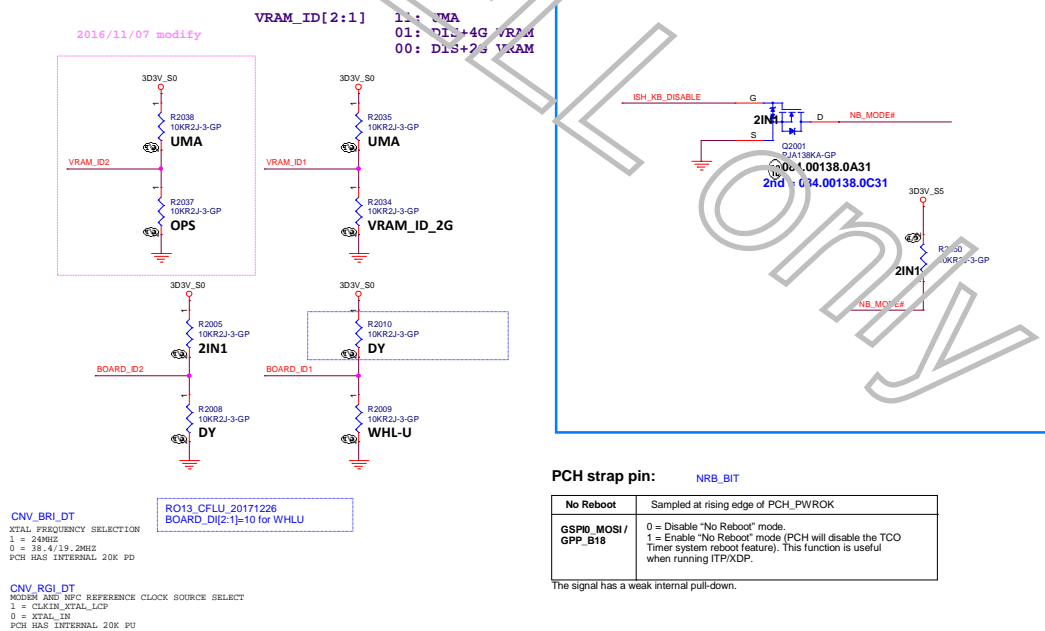
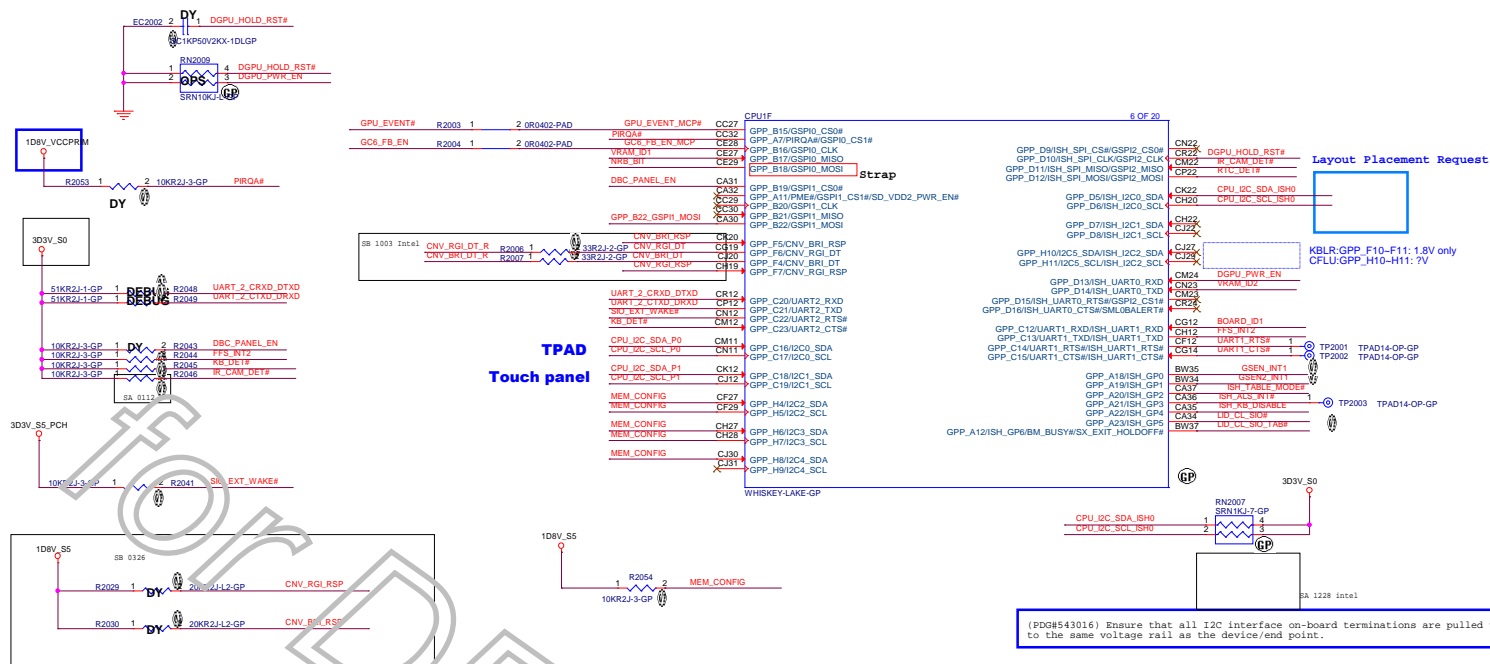
Strap	Usage	When Sampled	Comment
GP1_H0101 / GP1_H01	Root BIOS Strap	During start of POST/BIOS	This signal has a weak internal pull-down. This field determines the destination of access to the BIOS memory range. (Default: Accessing Root BIOS Destination at 0x00000000, Accessing Root BIOS at 0x00000000)
SMALERTP / GP1_CS	eSPI or LPC	During start of POST/BIOS	This signal has a weak internal pull-down. This signal is in the primary wall.

Timing diagram showing the relationship between the SD card signals and the processor signals. The signals are:

- SD_SDATA0
- SD_SDATA1
- SD_SDATA2
- SD_SDATA3
- SD_CMD
- SD_WP
- SD_CD_N
- SD_CLK
- SD_PWR_EN#

[illegible]

79.86		GCE_FB_EN	<<<	_____
55		GPU_C2_SDA_P1	<<<	_____
55		CPU_C2_SCL_P1	<<<	_____
55.66		CPU_C2_SDA_P0	<<<	_____
55.66		CPU_C2_SCL_P0	<<<	_____
55		DSC_PIXEL_EN	<<<	_____
68		UART_2_CTWD_DTWD	<<<	_____
68		UART_2_CTWD_DTWD	<<<	_____
24		SIO_EXT_WAKE#	<<<	_____
	65	IBO_DET#	<<<	_____
24.66.69		LIO_CL_SHD#	<<<	_____
	55	GSEN_INT1	>>>	_____
70		GSEN2_INT1	>>>	_____
	15.25	RTC_DET#	<<<	_____
55.70		CPU_C2_SDA_SH0	<<<	_____
55.70		CPU_C2_SCL_SH0	<<<	_____
	70	FFS_INT2	<<<	_____
91		PIRQA#	<<<	_____
21		BOARD_ID2	>>>	_____
	61	CNV_BRI_RSP	<<<	_____
	15.61	CNV_RGL_DT_R	<<<	_____
	61	CNV_BRI_DT_R	<<<	_____
	61	CNV_RGL_RST	<<<	_____
76		DGPU_HOLD_RST#	>>>	_____
79		GPU_EVENT#	>>>	_____
86		DGPU_PWR_EN	>>>	_____
15		NRB_BIT	>>>	_____
15		GPP_B22_GSPH1_MOSI	>>>	_____
24		NB_MODE#	>>>	_____
24.66.69		PAE_LC_SIO_TAR#	<<<	_____
24		ISH_TARI_F_MODE#	<<<	_____



NRB_BIT

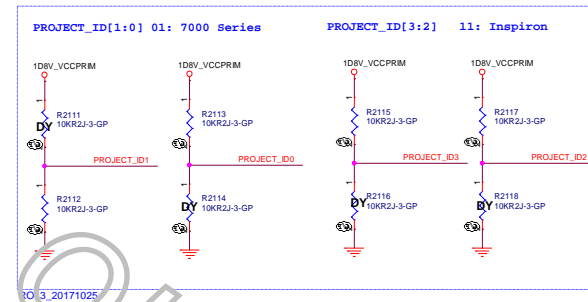
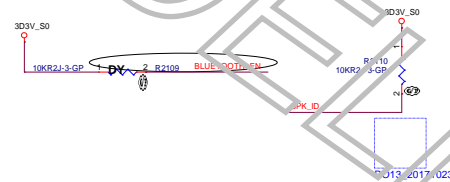
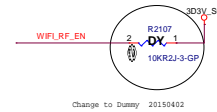
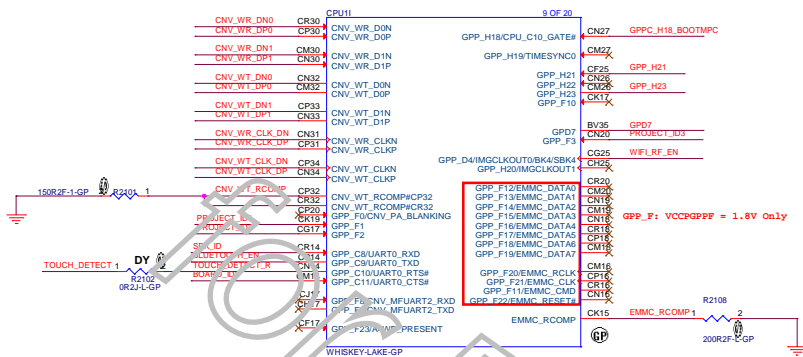
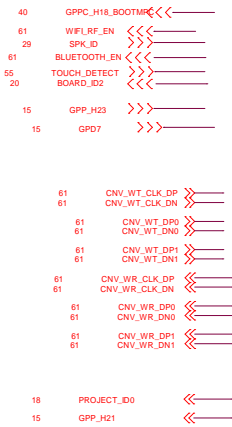
No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI/ GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

◀Core Design▶

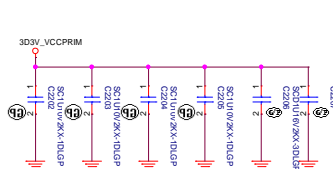
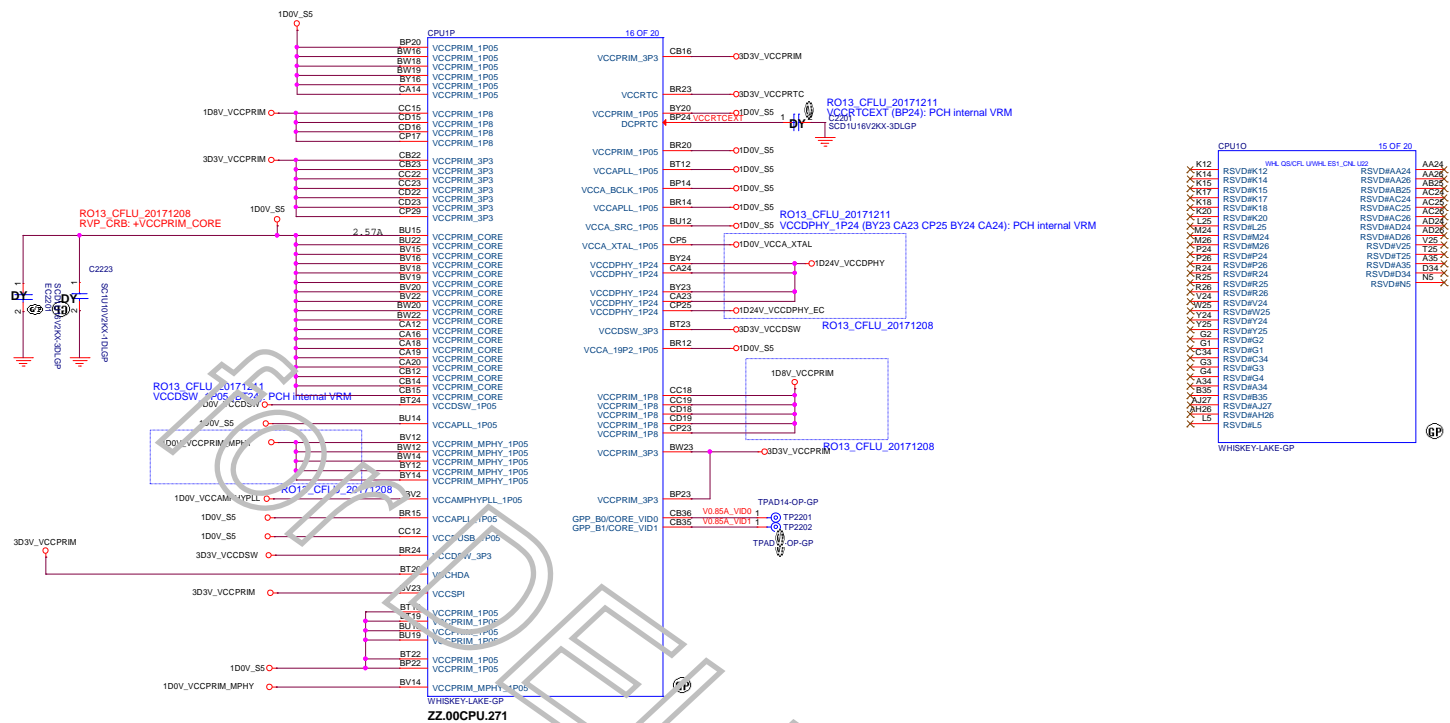


Main Func = PCH



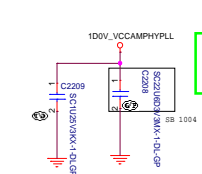
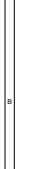
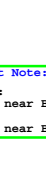
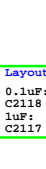
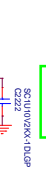
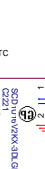
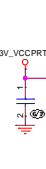
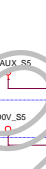
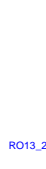
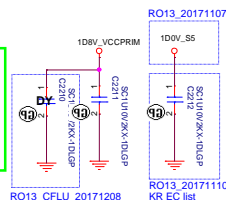
3D3V_VCCDSW

SC1U10V2K-1DGp
C2224

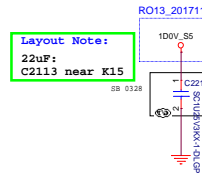


Layout Note:

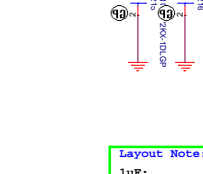
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19



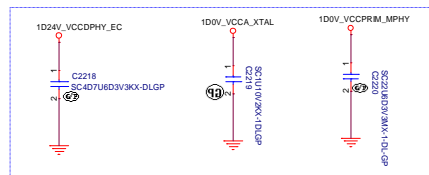
Layout Note:
22uF:
C2113 near BV2
C2126 near BV2



Layout Note:
22uF:
C2113 near K15



Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19



RO13_CFLU_20171208

Jedi UMA/DIS 2IN1

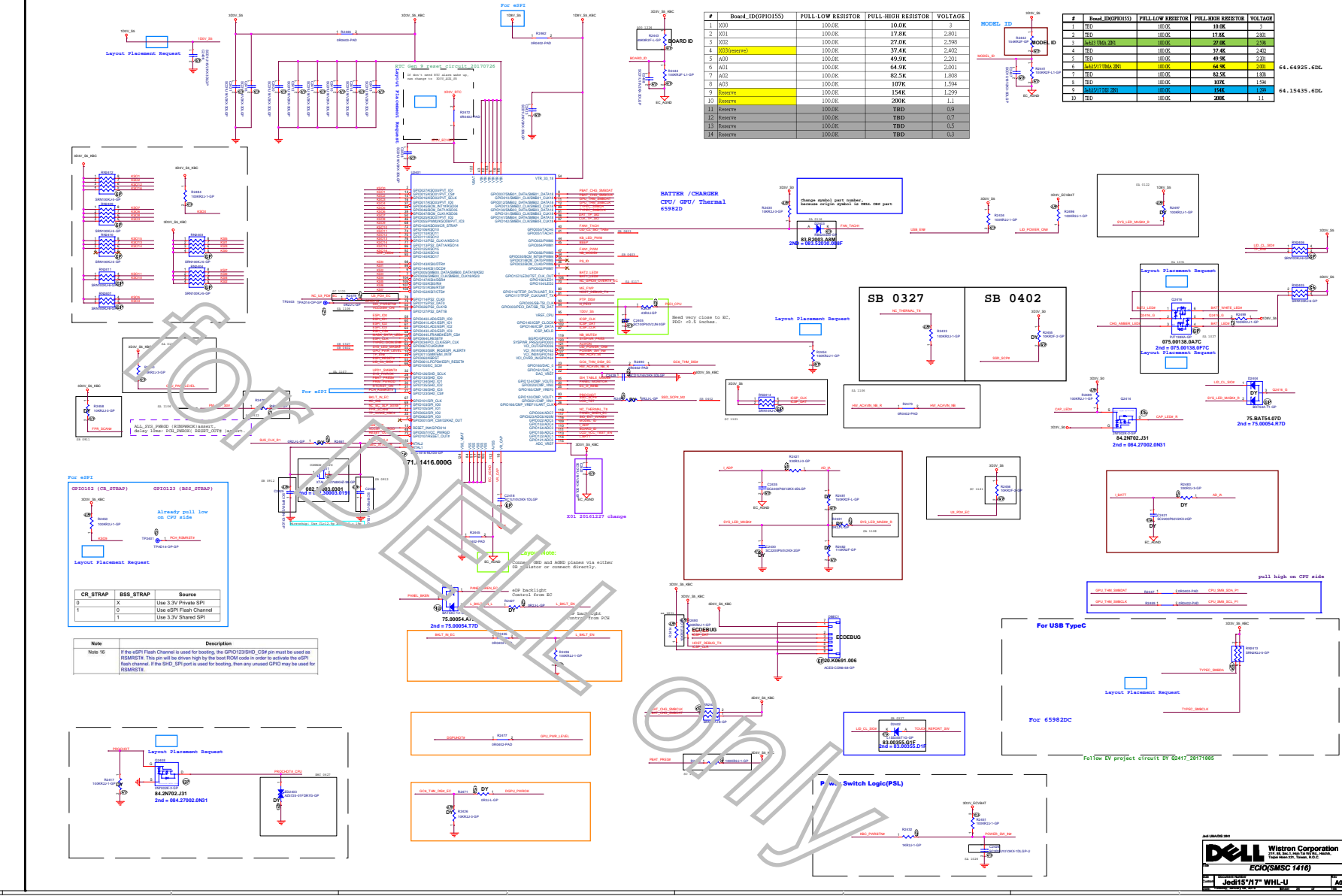
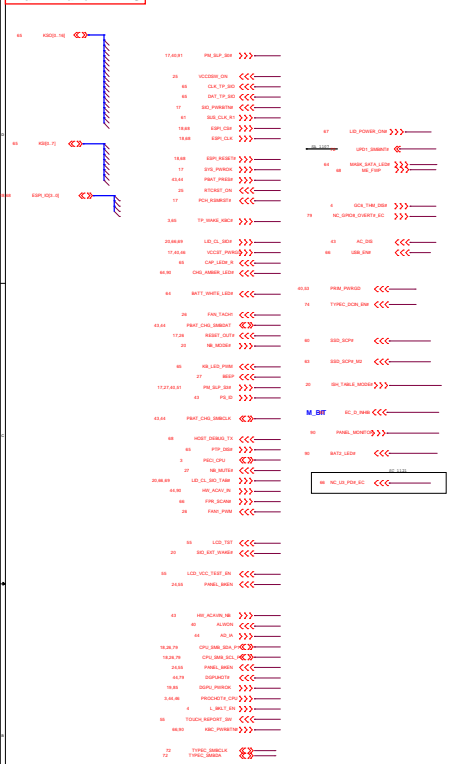


Title			
CPU (PCH-LP PWR&Caps)			
Size	Document Number	Rev	
A2	Jedi15"/17" WHL-U	A00	
Date:	Tuesday, January 08, 2019	Sheet	22 of 106



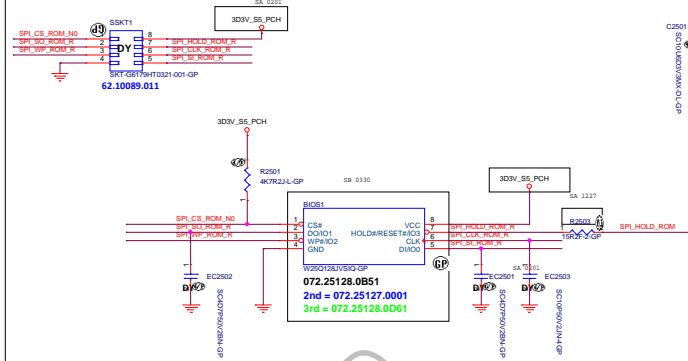
1

1



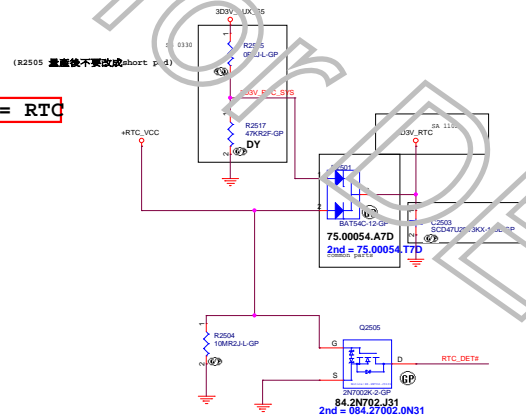
Main Func = SPI Flash

SPI Flash ROM(16M) for PCH



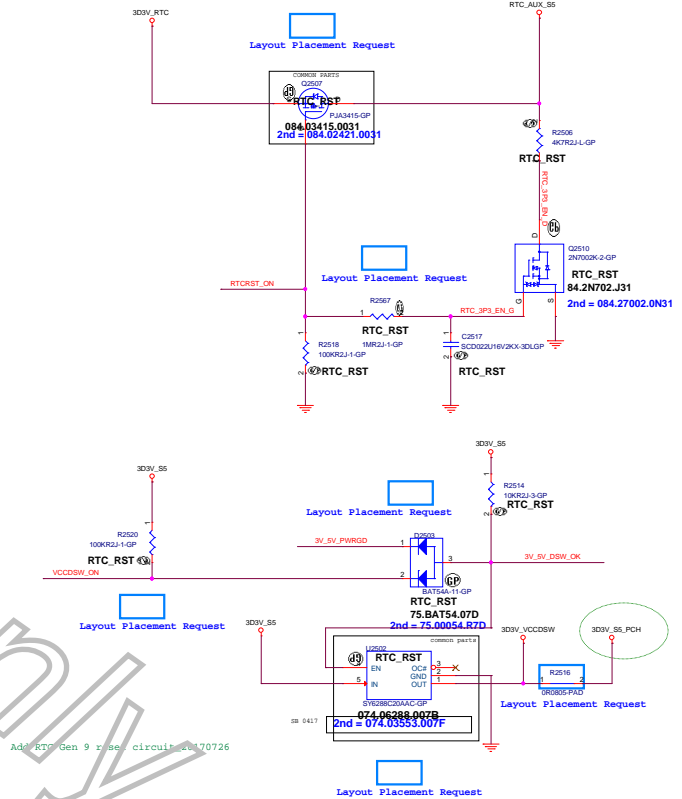
Source	QUAD/DUAL fast read	DUAL fast read	SFDP
072.25128.0051	0	0	0
072.25127.0001	0	0	0
072.25128.0061	0	0	0

Main Func = RTC



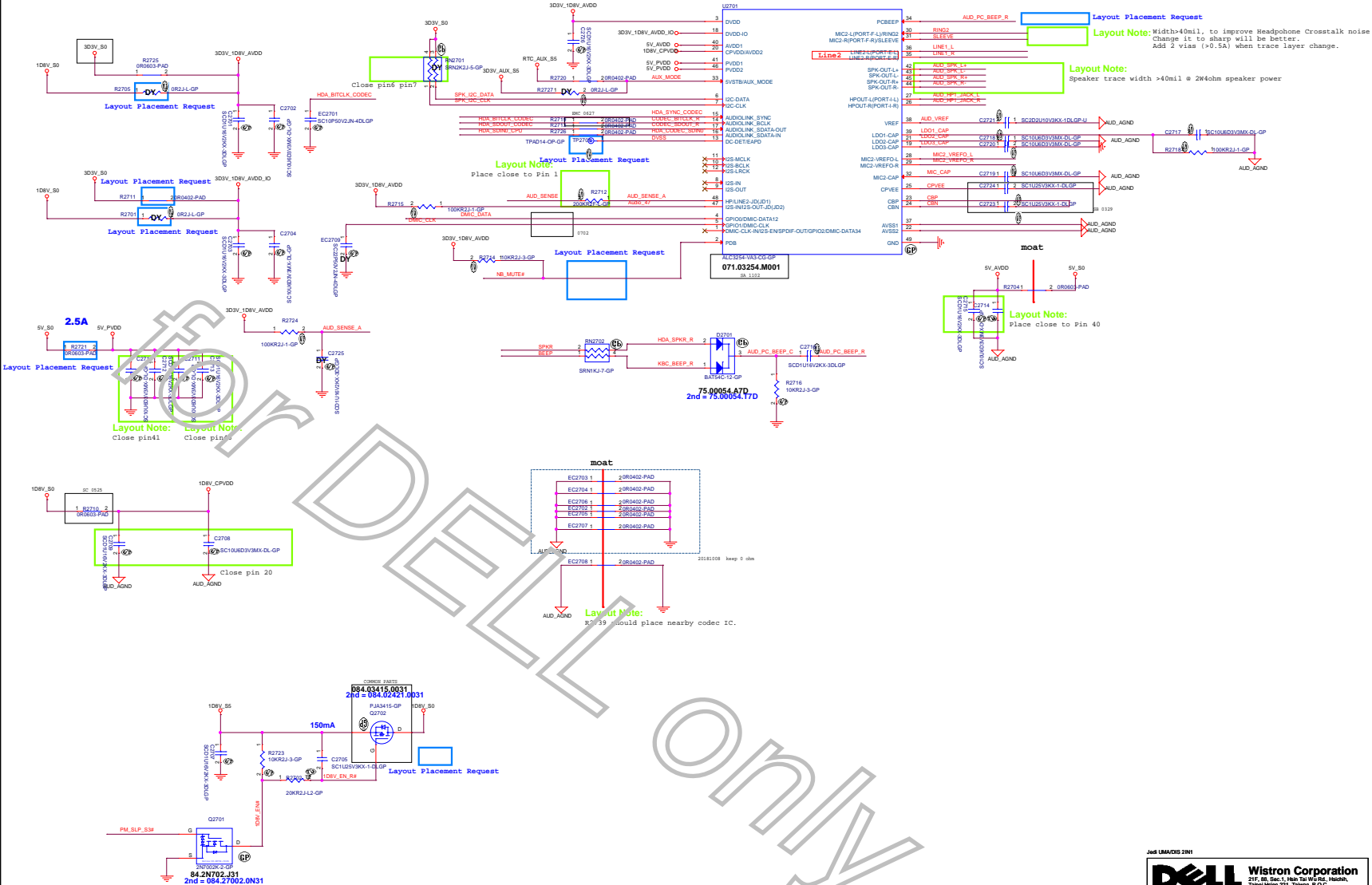
29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



Main Func = Audio

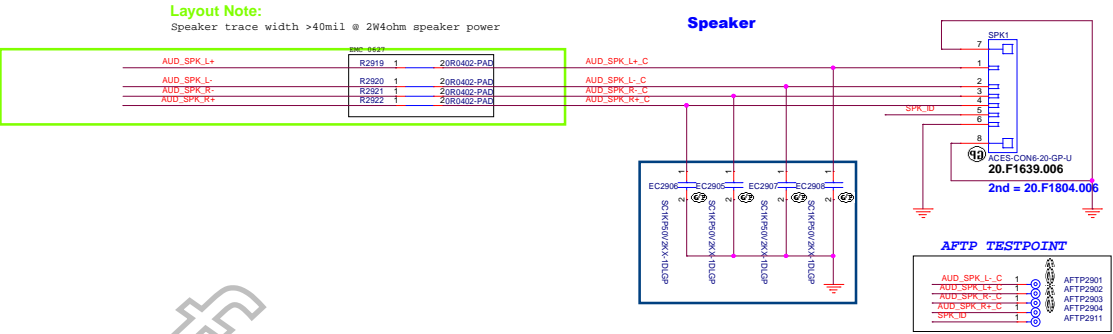
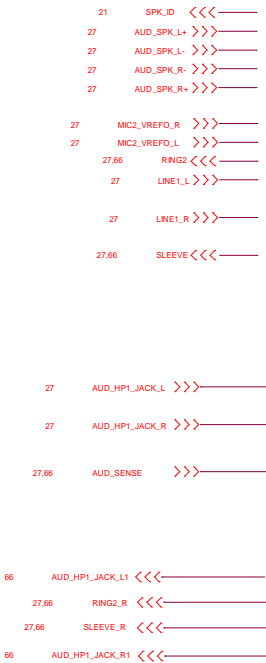
19	HDA_SYNC_CODEC	>>>
19	HDA_IDOUT_CODEC	>>>
55	DMIC_DATA	<<<
66	AUD_SENSE	<<<
19	HDA_SNDNG_CFS	<<<
55	DMIC_CLK	<<<
24	DMIC	<<<
29.66	RING2	>>>
15.19	SPKR	>>>
29	LINE1_L	>>>
29	LINE1_R	>>>
24	NB_MUTEF	>>>
29	AUD_SPK_L+	<<<
29	AUD_SPK_L-	<<<
29	AUD_SPK_R+	<<<
29	AUD_SPK_R-	<<<
29	AUD_HP1 JACK_L	<<<
29	AUD_HP1 JACK_R	<<<
29	MC12_VREFIO_L	<<<
29	MC12_VREFIO_R	<<<
29.66	SLEEVE	>>>
17.40.51	PM_SLP_S34	>>>



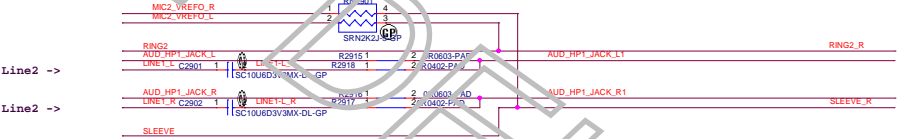
(Blanking)

for DELL only

Main Func = Audio



for DELL only



for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio (RSVD)

Size

A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date:

Tuesday, January 08, 2019

Sheet

1

30

of

106

(Blanking)

for DELL only

(Blanking)

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN (RSVD) (RJ45+Transformer)

Size
A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 32 of 106

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB2.0 CONN)

Size
A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 34 of 106

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB3.0 Conn)

Size

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 35 of 106

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB Charger)

Size
A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 36 of 106

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (PCIE to USB3.0)

Size
A4

Document Number

Jedi15"/17" WHL-U

Rev
A00

Date: Tuesday, January 08, 2019

Sheet 37 of 106

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB3.0 Redriver)

Size
A4

Document Number

Jedi15"/17" WHL-U

Rev
A00

Date: Tuesday, January 08, 2019

Sheet 38 of 106

for DELL only

Jedi UMA/DIS 2N1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshan, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Sequence (RSVD)			
Size	Document Number	Rev	
A2	Jedi15"/17" WHL-U	A00	
Date: Tuesday, January 08, 2019		Sheet	39 of 106

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sequence (RSVD) (DS3/S0ix)

Size
A4

Document Number

Jedi15"/17" WHL-U

Rev
A00

Date: Tuesday, January 08, 2019

Sheet 41 of 106

for DELL only

Jedi UMA/DIS 2N1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshien,
Taipei Hsien 221, Taiwan, R.O.C.

Title **INT IO (RSVD)**

Size A2	Document Number Jedi15"/17" WHL-U	Rev A00
------------	---	-------------------

Date: Tuesday, January 08, 2019 Sheet 42 of 106

24 HW_ACAVIN_NB <<<—

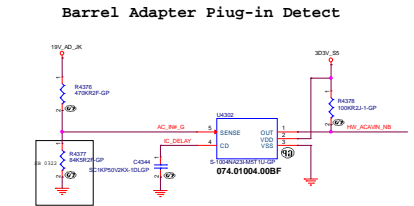
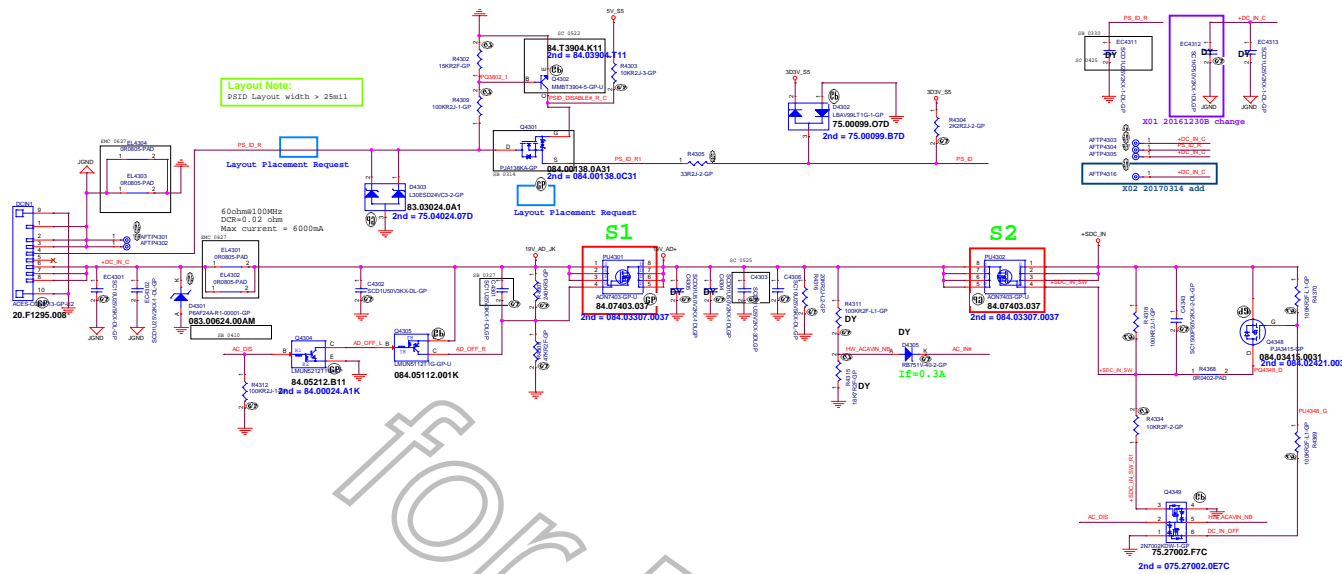
24 PS_ID <<<—

24 AC_Bn AC_DIS >>>—

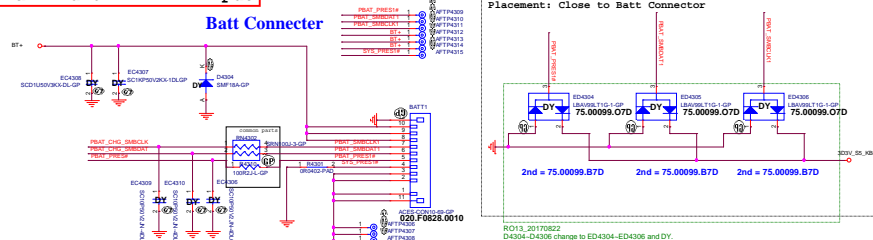
24,44 PBAT_CHG_SMBCLK >>>—

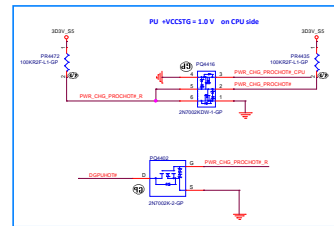
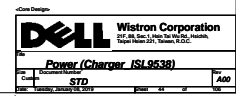
24,44 PBAT_CHG_SMBDAT >>>—

24,44 PBAT_PRES# >>>—



Batt Connector

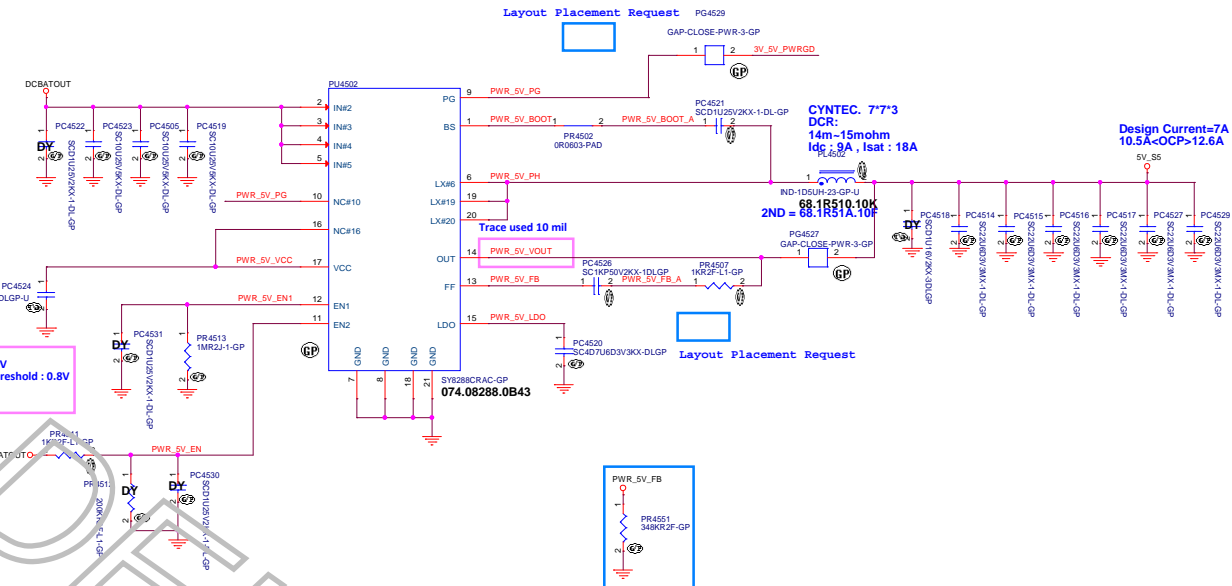
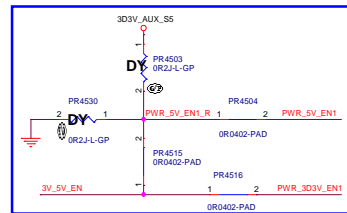


[illegible][illegible]

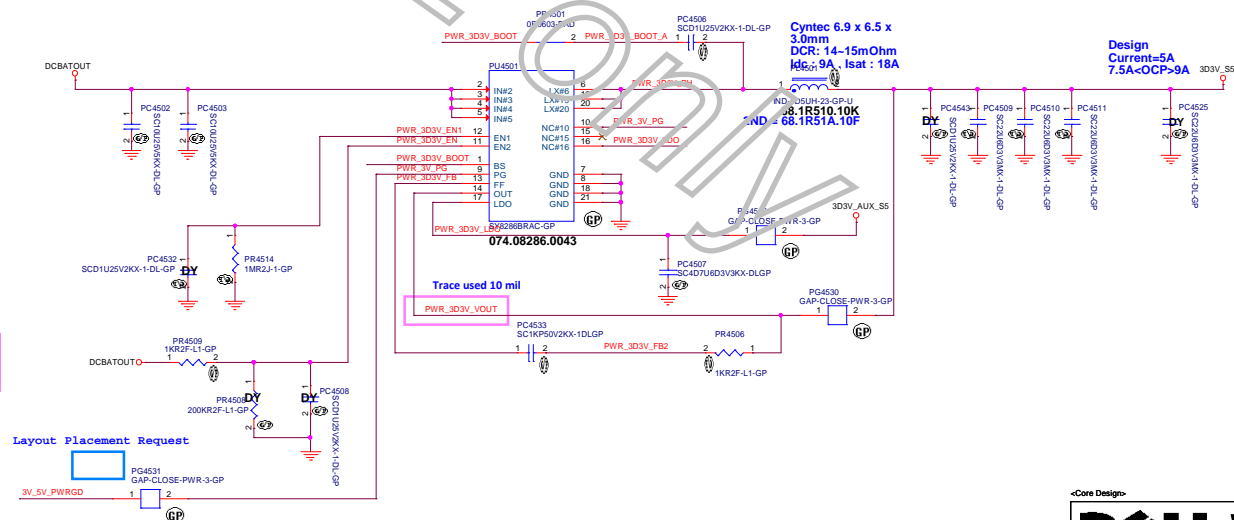
Main Func = PWR.Plane.Regulator_5V

OFFPAGE-Signal

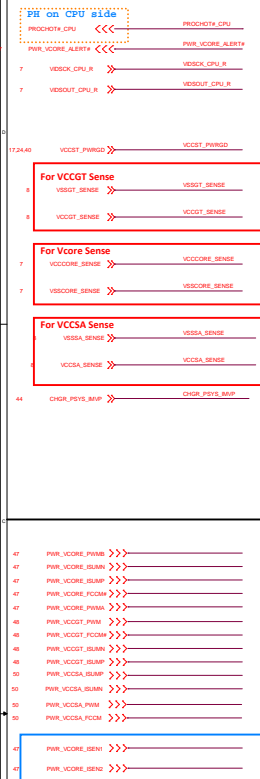
OFFPAGE-GAP



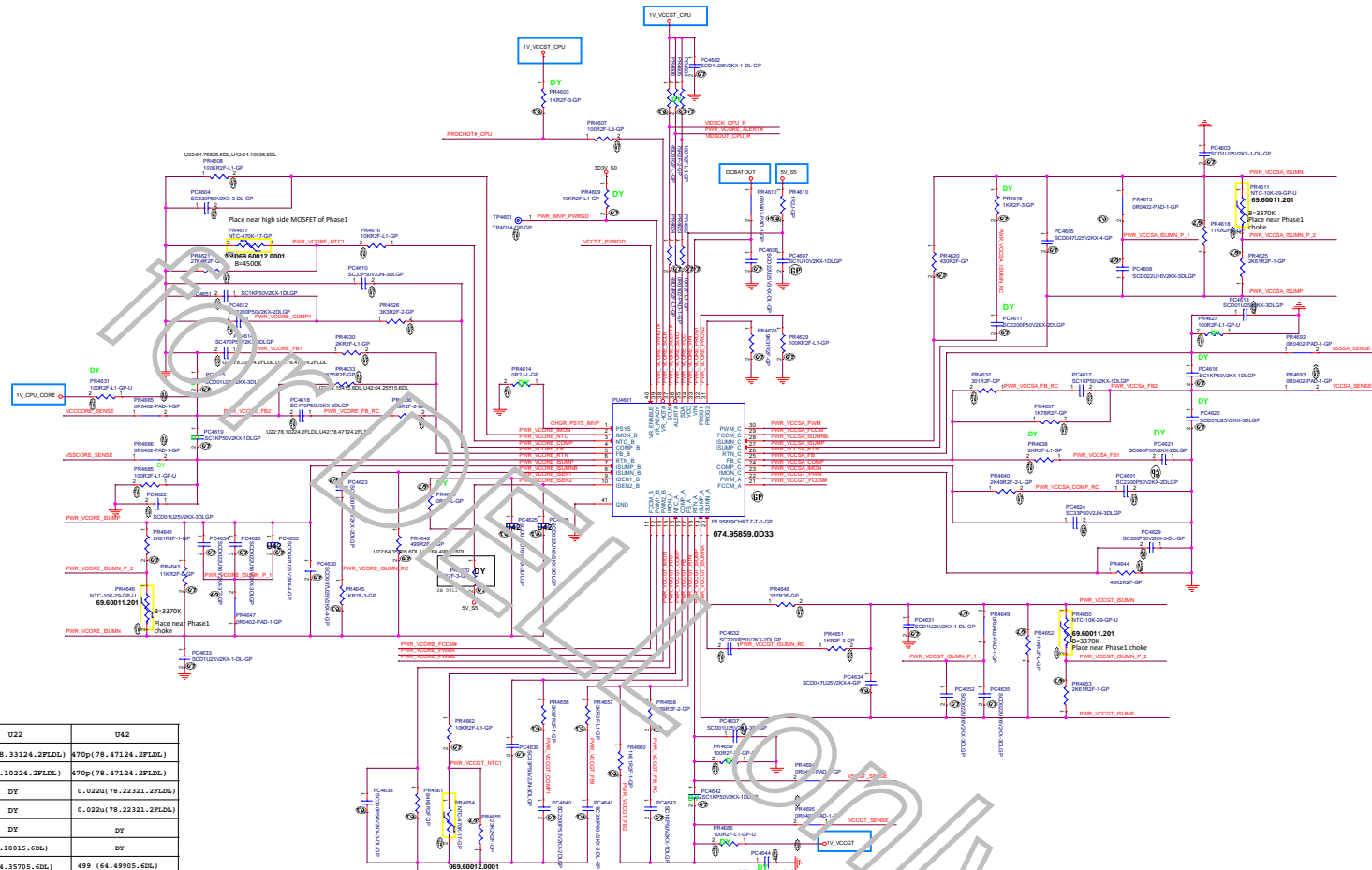
Main Func = PWR.Plane.Regulator_3D3V

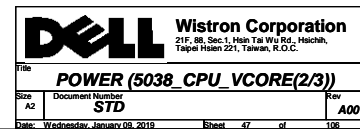


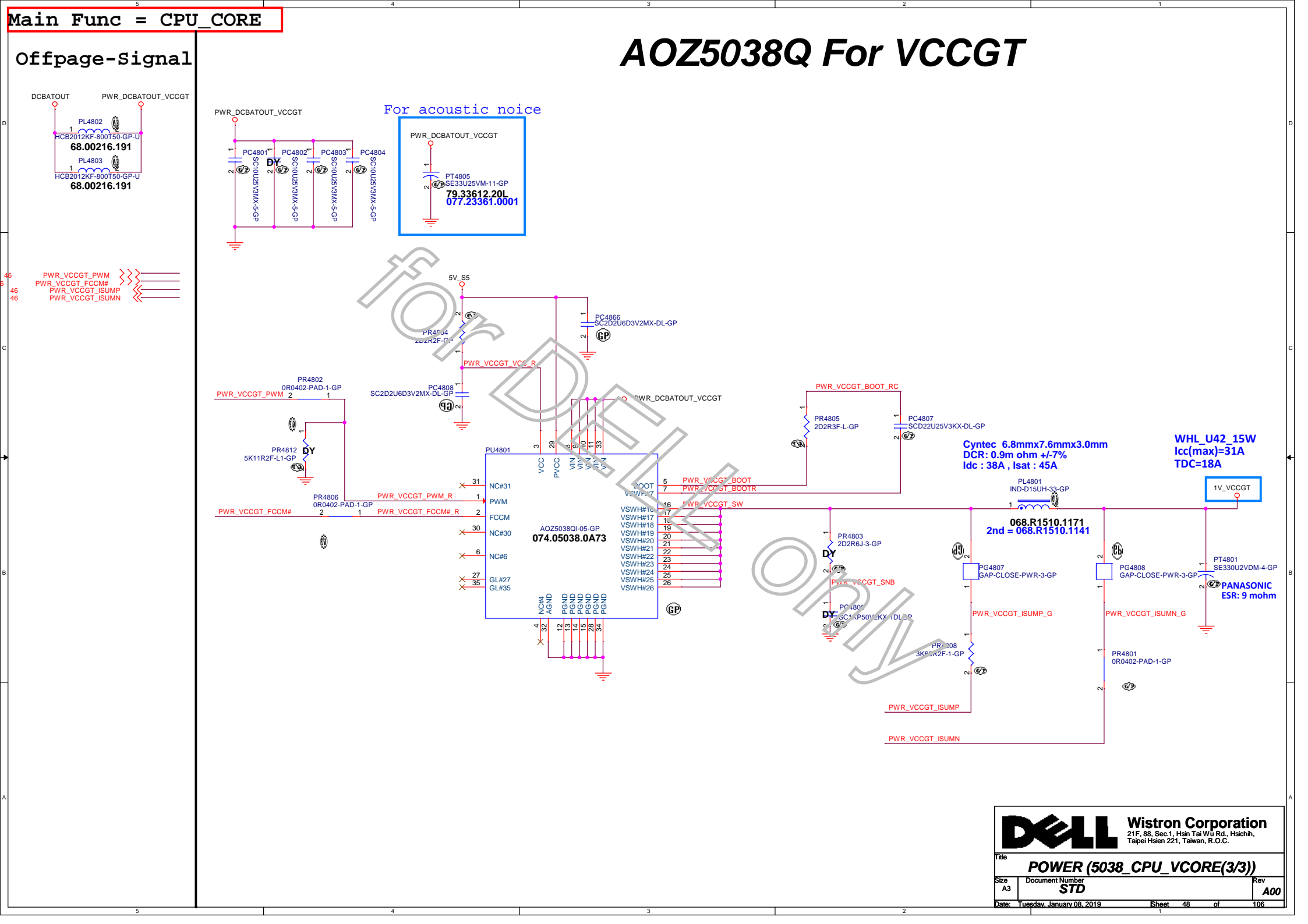
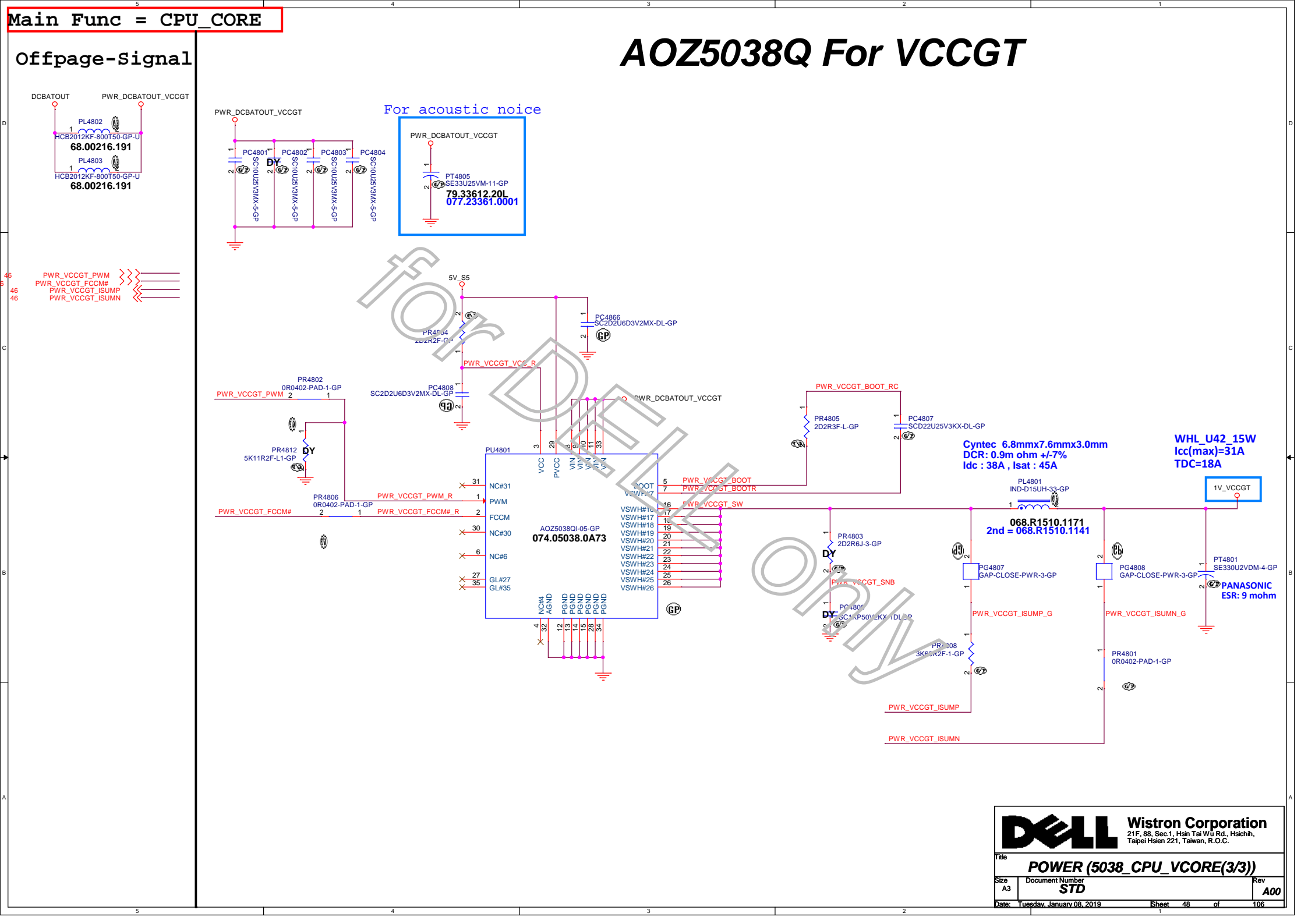
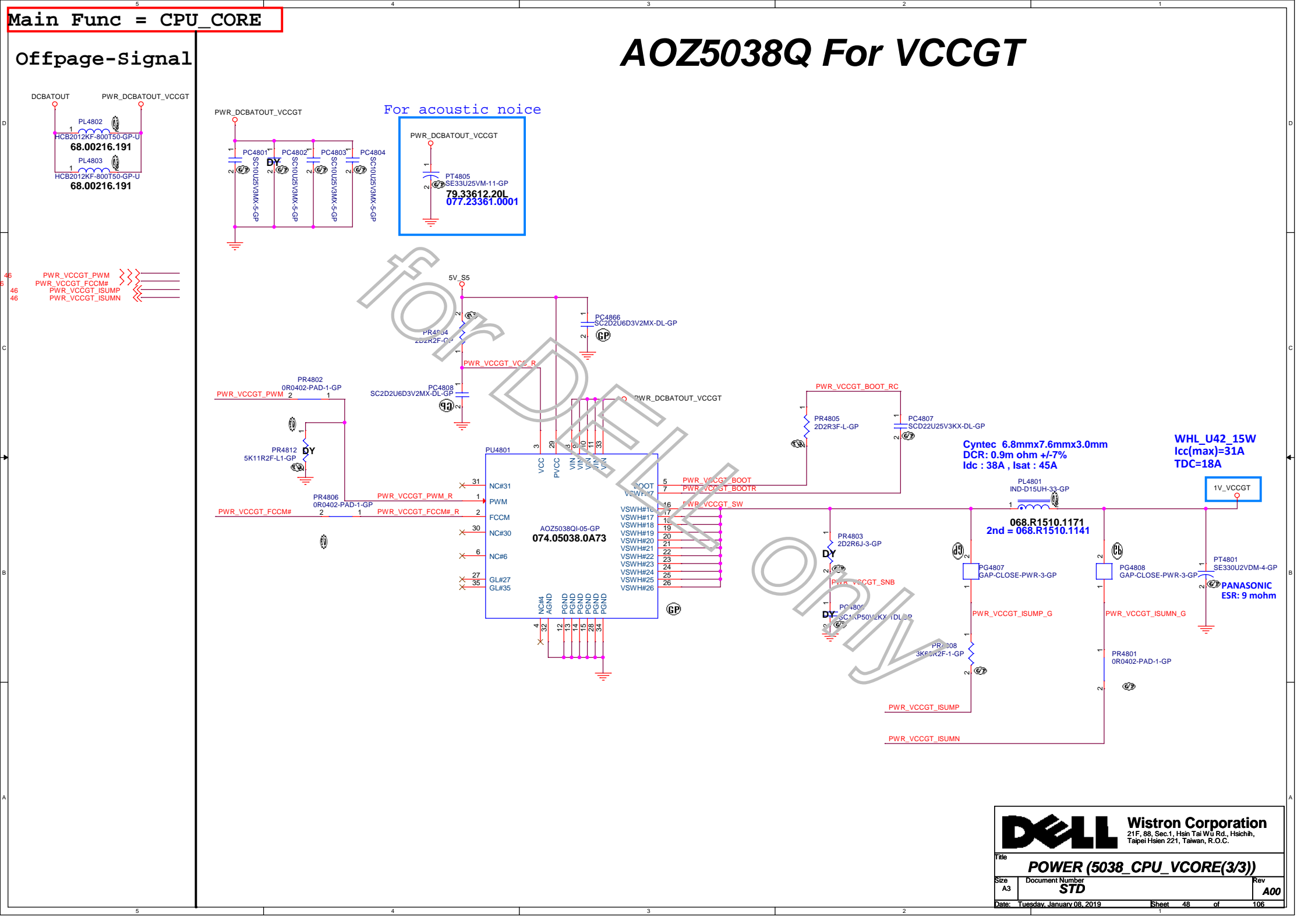
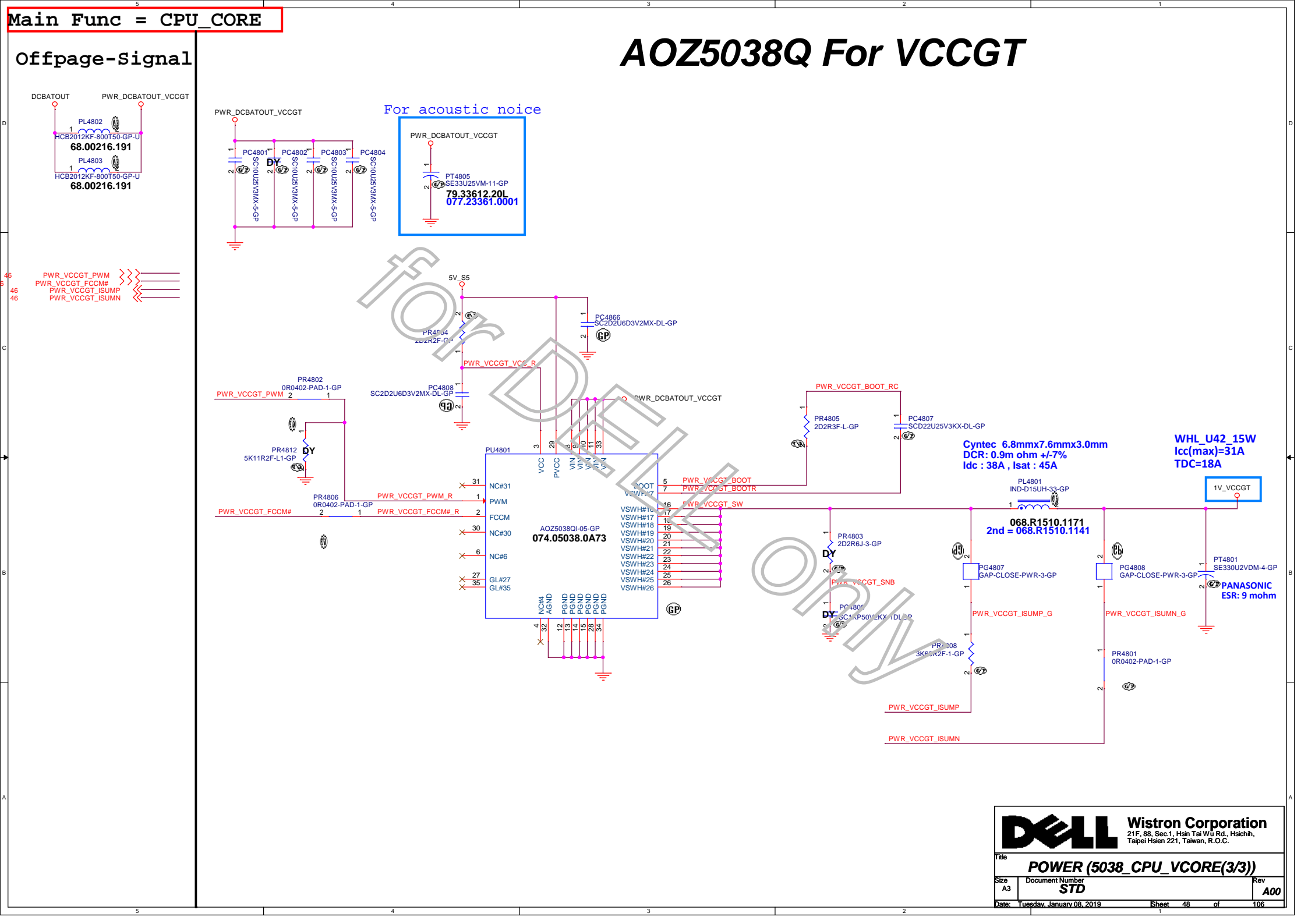
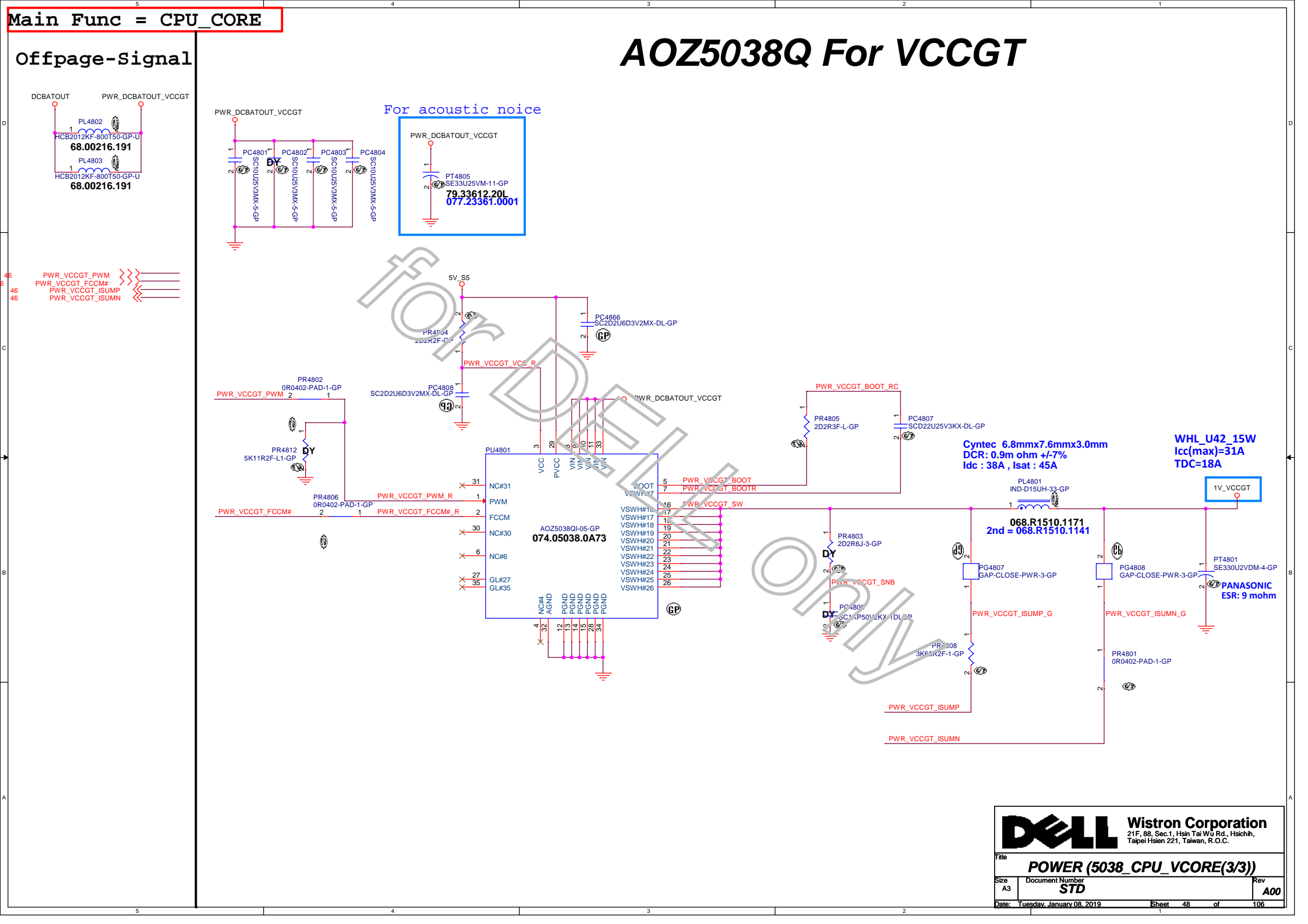
<Core Design>



	U22	U42
PC4614	330P(78.33124,2FL6L)	470P(78.47124,2FL6L)
PC4618	1KP(78.10224,2FL6L)	470P(78.47124,2FL6L)
PC4625	DY	0.022u(78.22321,2FL6L)
PC4626	DY	0.022u(78.22321,2FL6L)
PR4669	DY	DY
PR4635	1K1(64.10015,6DL)	DY
PR4642	357(64.35705,6DL)	489(64.49905,6DL)
PC4640	47uP(078.47322,02PD)	47uP(078.47322,02PD)
PC4628	22uP(78.22321,2FL6L)	22uP(78.22321,2FL6L)
PC4654	15uP(78.10324,2FL6L)	22uP(78.22321,2FL6L)
PC4653	DY	47uP(078.47322,02PD)
PR4631	1.54K(64.15415,6DL)	2.55K(64.25515,6DL)
PR4608	76.8K(64.76825,6DL)	100K(64.10005,6DL)





[illegible][illegible][illegible]

for DELL only

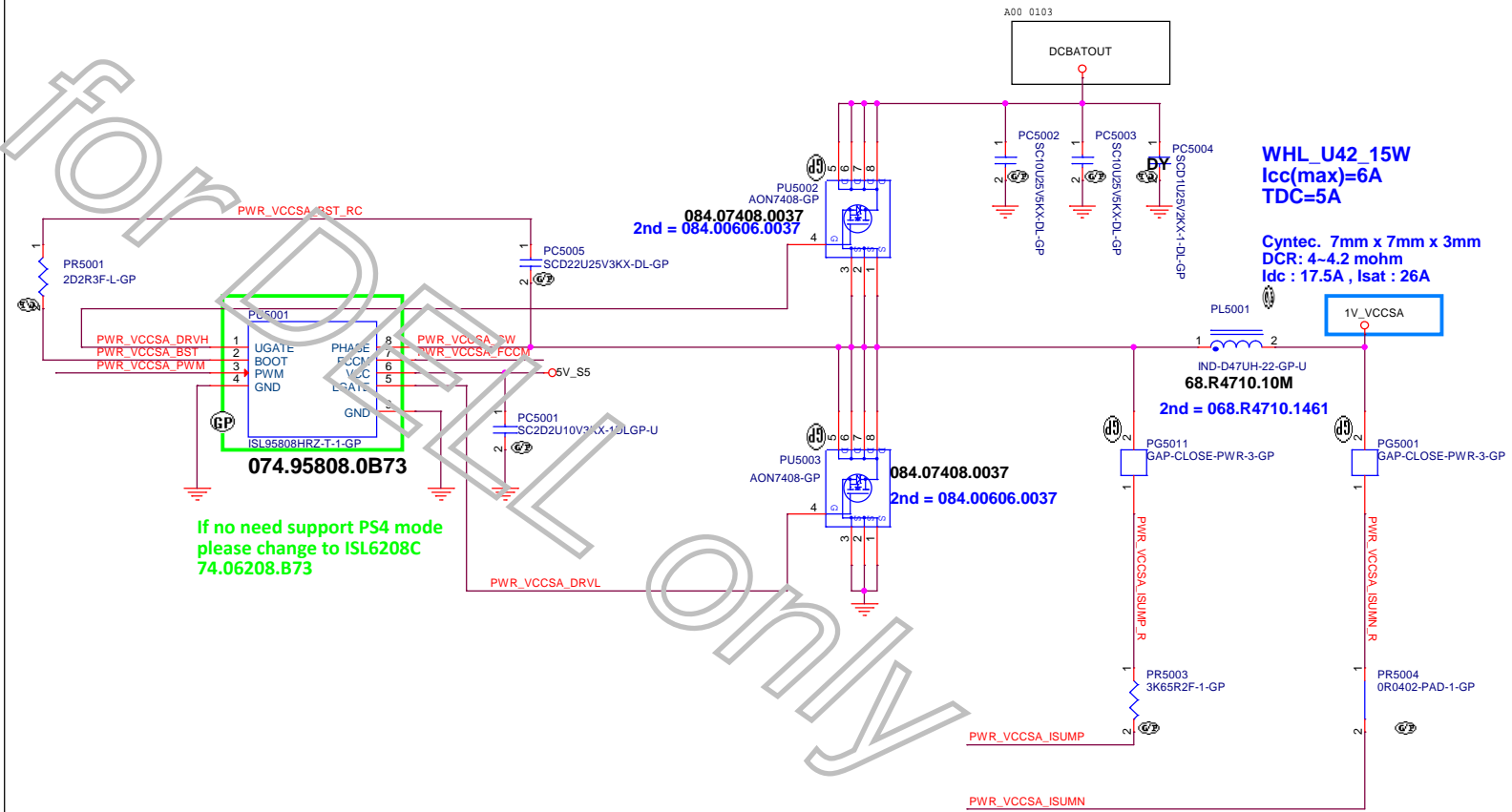
Main Func = CPU_CORE

OFFPAGE-Signal

PWR_VCCSA_PWM >>>—
PWR_VCCSA_ISUMP <<<—
PWR_VCCSA_ISUMN <<<—
PWR_VCCSA_FCCM >>>—

OFFPAGE-GAP

A00 0103



<Core Design>

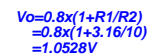
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VCCSA**

Size: A3 Document Number: **Jedi15"/17" WHL-U** Rev: **A00**

Date: Wednesday, January 09, 2019 Sheet: 50 of 106

3V_5V_DSW_OK >>> _____



Title			
(Reserved)			
Size	Document Number		Rev
Custom	Jedi15"/17" WHL-U		A00
Date:	Tuesday, January 08, 2019	Sheet 52 of	106

Main Func = 1D8V

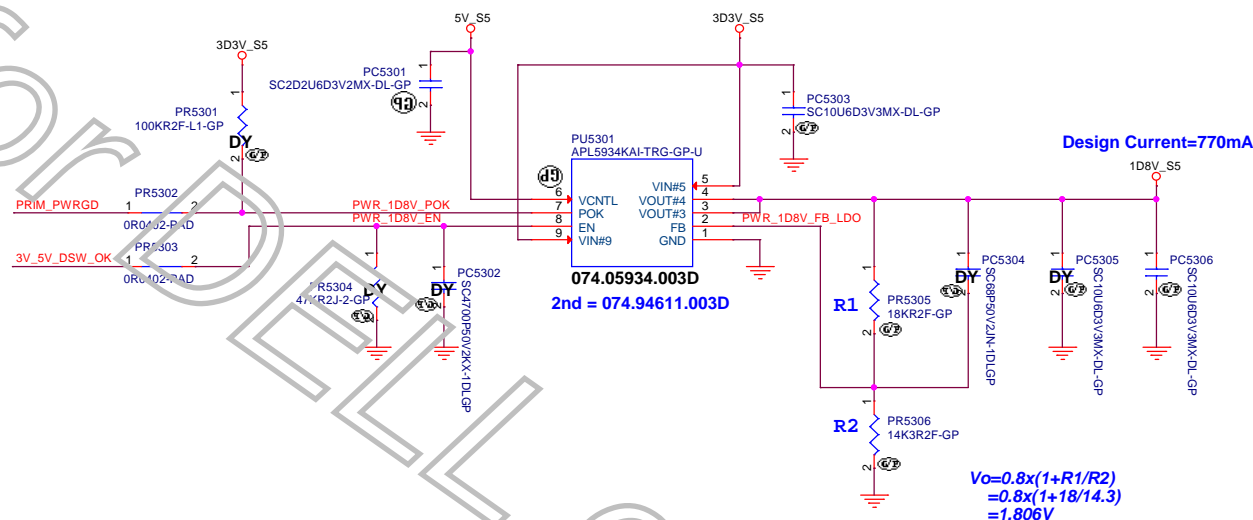
OFFPAGE-Signal

OFFPAGE-GAP

PRIM_PWRGD <<<

3V_5V_DSW_OK >>>

APL5934 for 1D8V_S5



<Core Design>




Title			(Reserved)
Size	Document Number	Rev	
A3	Jedi15"/17" WHL-U	A00	
Date:	Tuesday, January 08, 2019	Sheet	53 of 106

Main Func = 2D5V/ 1D8V

for DELL only

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date:

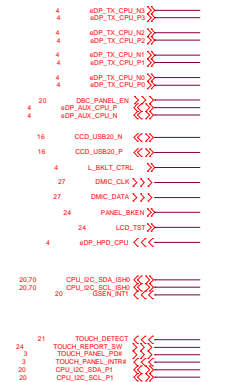
Tuesday, January 08, 2019

Sheet

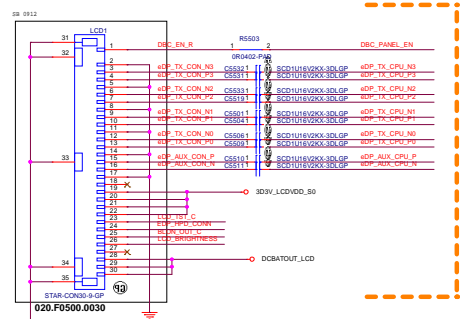
54

of

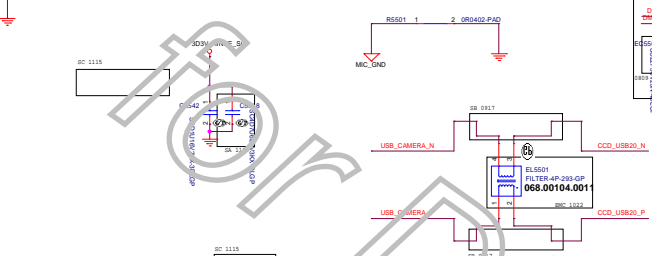
106



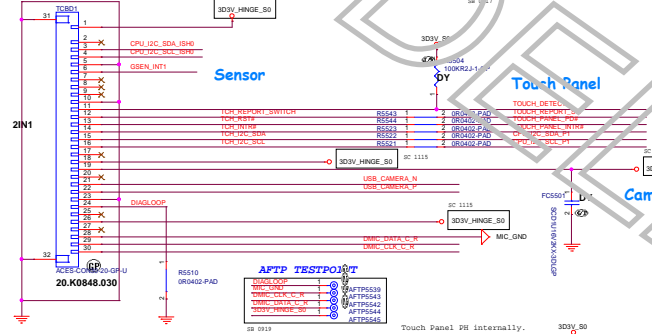
Panel / Camera/ DMIC



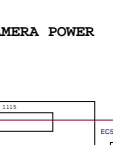
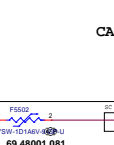
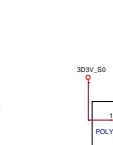
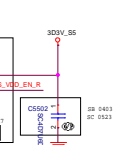
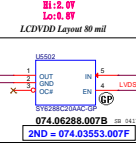
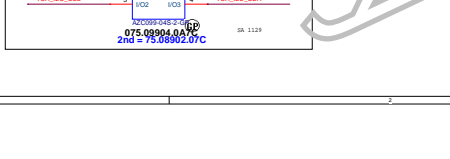
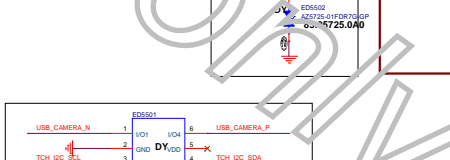
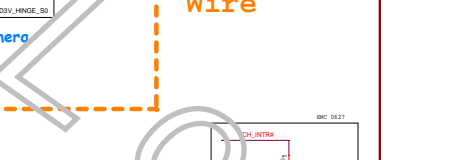
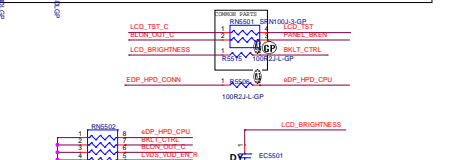
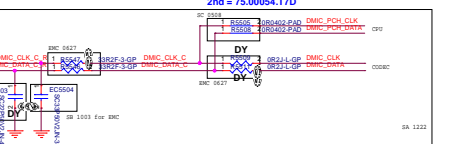
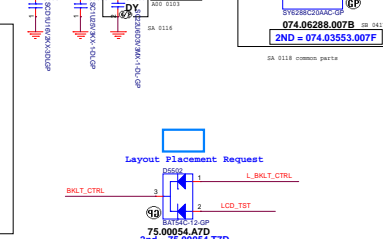
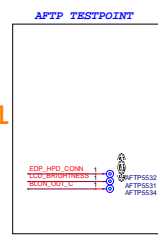
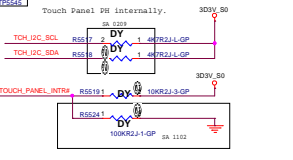
Coaxial



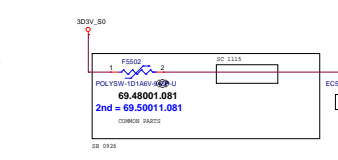
Wire



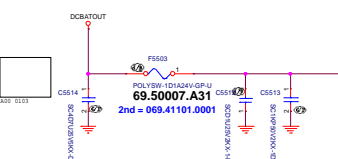
TP	PIN	DEFINE
1	VUSB_3.3V	
2	NC	
3	SCL	
4	SDA	
5	UA_INT	
6	RESET	
7	Report Switch	
8	NC	
9	GND	
10	GND	



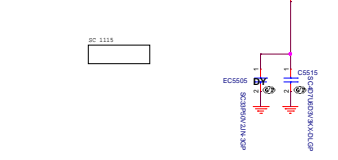
CAMERA POWER



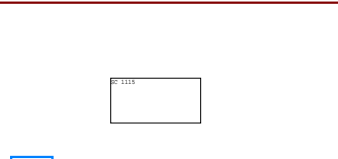
INVERTER POWER



SENSOR POWER

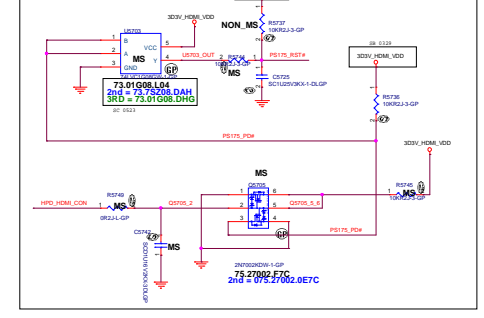
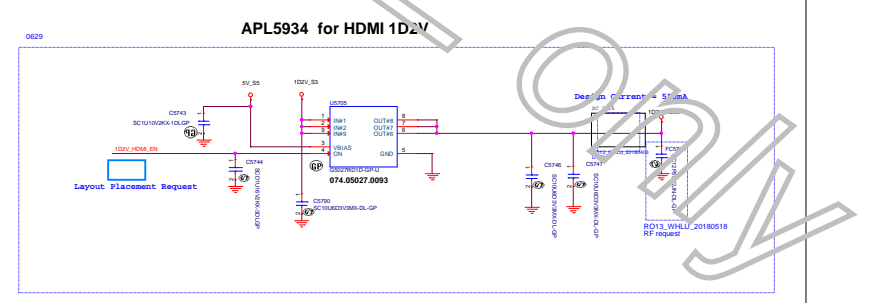
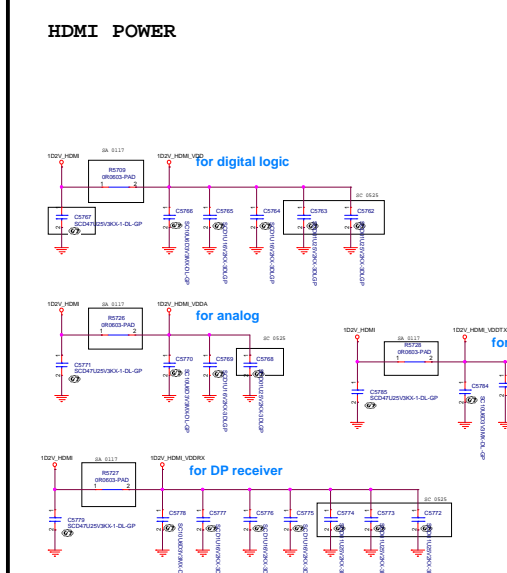
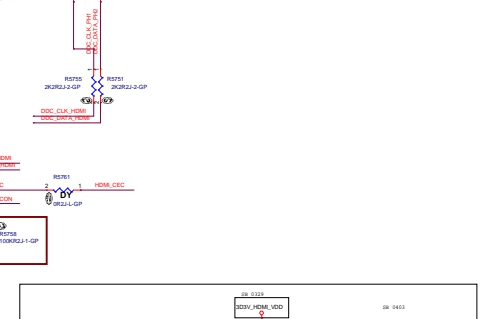
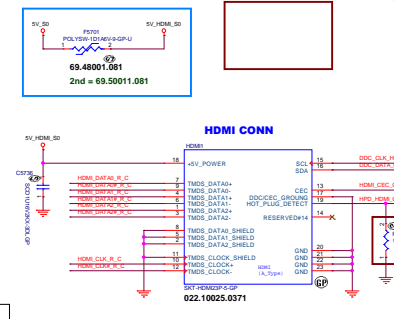
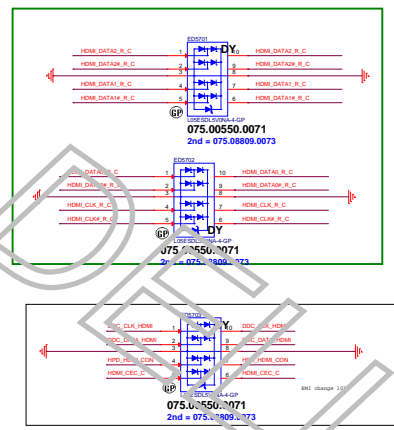
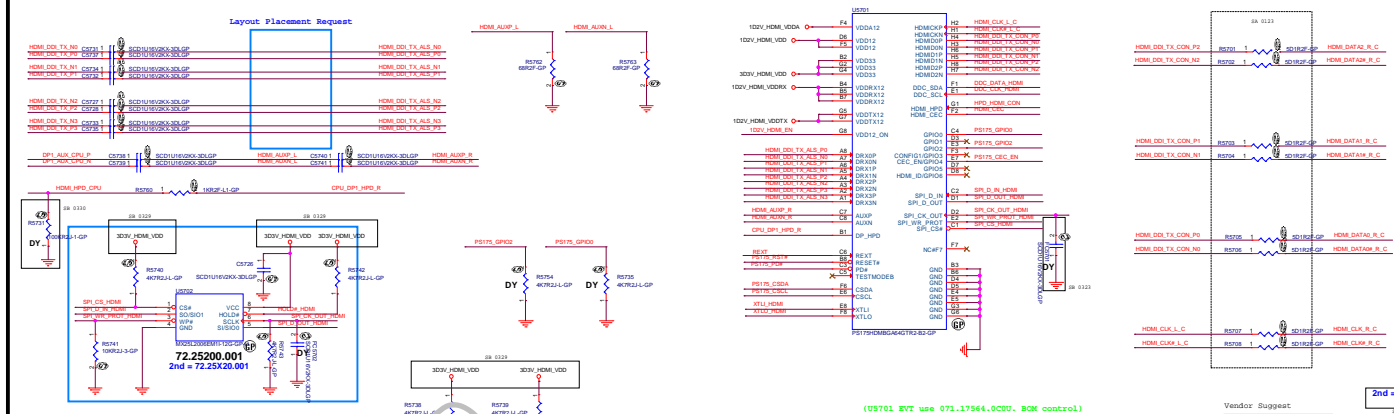
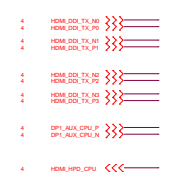


TOUCH PANEL POWER



for DELL only

Main Func = HDMI



for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		Display (RSVD) DP	
Size	Document Number	Rev	
Custom	Jedi15"/17" WHL-U	A00	
Date: Tuesday, January 09, 2019		Sheet	58 of 106

for DELL only

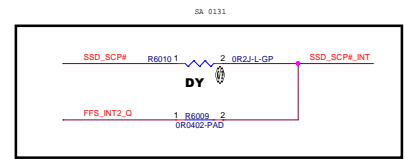
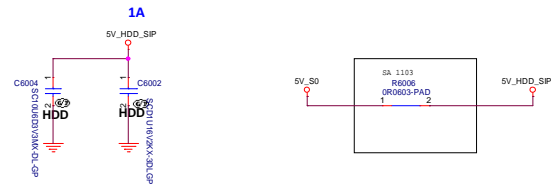
(Blanking)

Jedi UMA/DIS 2IN1

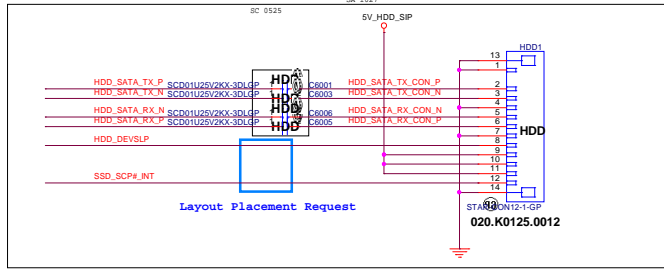


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

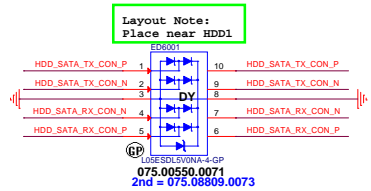
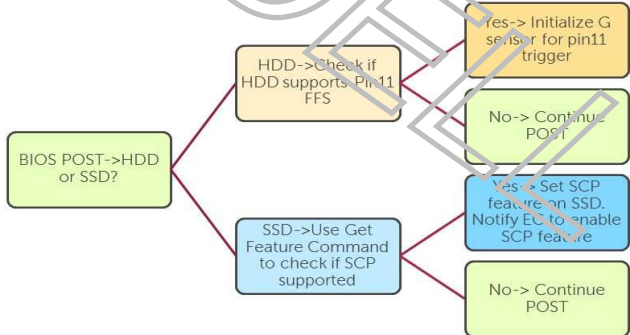
Title		
Display (RSVD) DVI		
Size	Document Number	Rev
A3	Jedi15"/17" WHL-U	A00
Date:	Tuesday, January 08, 2019	Sheet 59 of 106



SATA HDD Connector



- BIOS today already check whether the device is HDD and whether it supports FFS before enabling sensor chip to trigger pin11. The plan is to add a check on the SSD path to decide if device supports SCP and notify EC whether to support SCP.

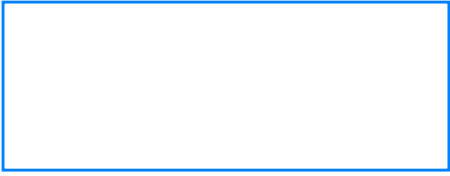
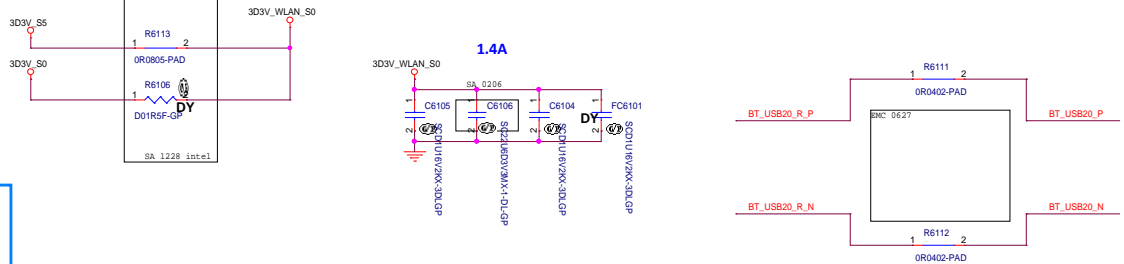


Main Func = WLAN

3.3 Peak current consumption

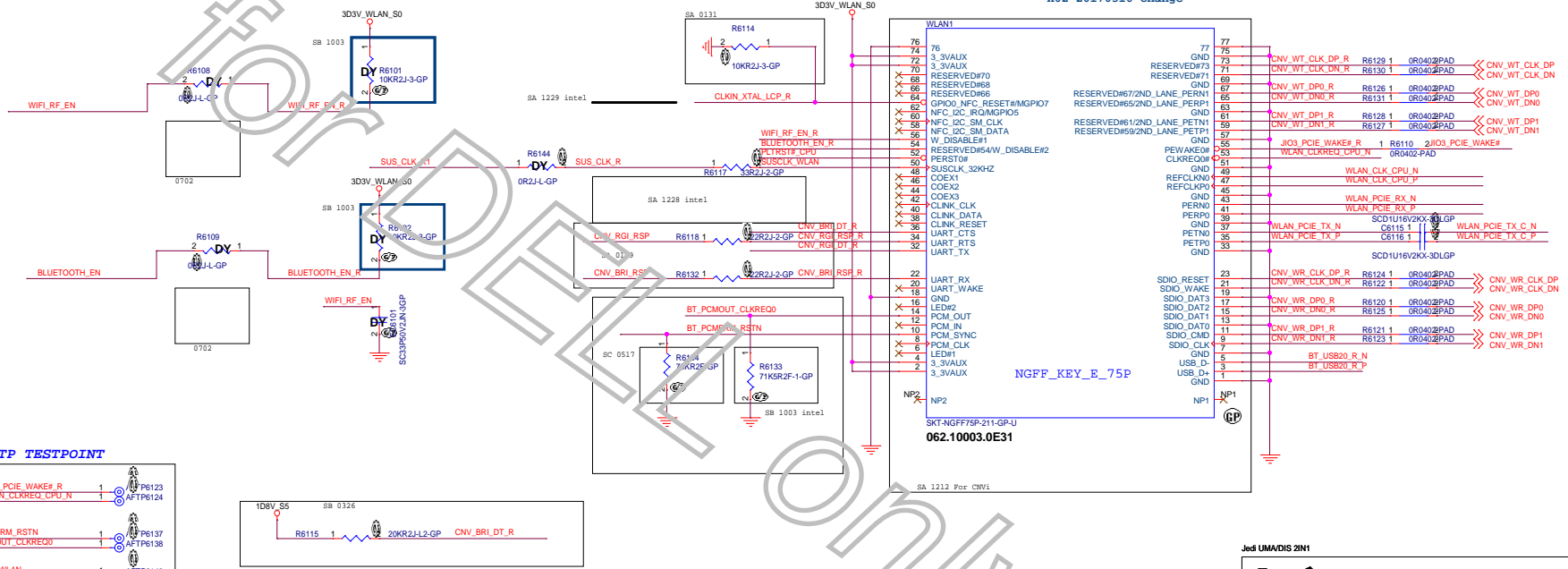
Table 3-4 Peak current consumption

Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply	1360	



Layout Placement Request

- BT_USB20_P <<>>
- BT_USB20_N <<>>
- WIFI_RF_EN >>>>
- WLAN_PCIE_TX_C_N >>>>
- WLAN_PCIE_TX_C_P >>>>
- PLTRST#_CPU >>>>
- BLUETOOTH_EN >>>>
- WLAN_CLKREQ_CPU_N <<>>
- WLAN_CLK_CPU_N >>>>
- WLAN_CLK_CPU_P >>>>
- WLAN_PCIE_RX_N <<>>
- WLAN_PCIE_RX_P <<>>
- CLKIN_XTAL_LCP_R >>>>
- BT_PCMOUT_CLKREQ0 >>>>
- BT_PCMFRM_RSTN >>>>
- JIO3_PCIE_WAKE# >>>>
- SUS_CLK_R1 >>>>
- SUS_CLK_R >>>>
- CNV_RGL_RSP <<>>
- CNV_BRI_RSP <<>>
- CNV_BRI_DT_R <<>>
- CNV_RGL_DT_R <<>>



AFTP TESTPOINT

JIO3_PCIE_WAKE#_R	1	P6123
WLAN_CLKREQ_CPU_N	1	AFTP6124
BT_PCMFRM_RSTN	1	P6137
BT_PCMOUT_CLKREQ0	1	AFTP6138
SUSCLK_WLAN	1	AFTP6143
3D3V_WLAN_S0	1	P6113
PLTRST#_CPU	1	P6108
WIFI_RF_EN_R	1	P6110
BLUETOOTH_EN_R	1	AFTP6112

Jed UMADIS 2N1

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (WLAN M.2)**

Size: Custom Document Number: **Jedi15"/17" WHL-U** Rev: **A00**

Date: Tuesday, January 08, 2019 Sheet: 61 of 106

for DELL only

(Blanking)

Jedi UMA/DIS 2IN1



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (RSVD) WWAN

Size
A4

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 62 of 106

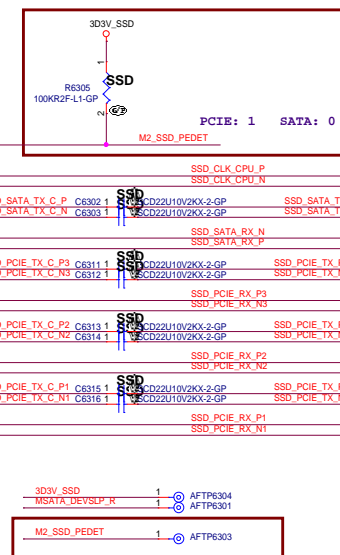
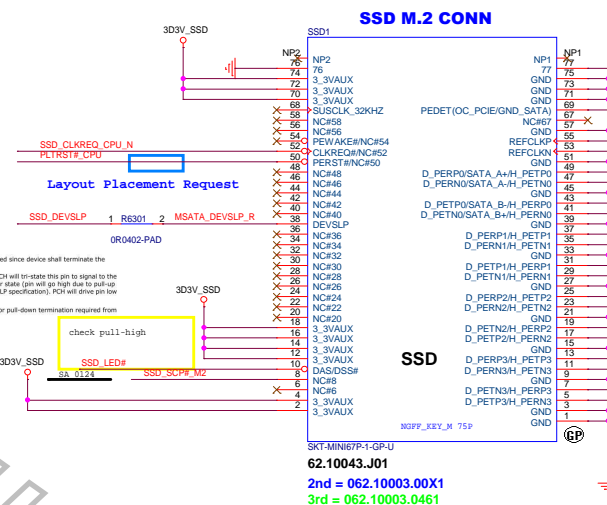
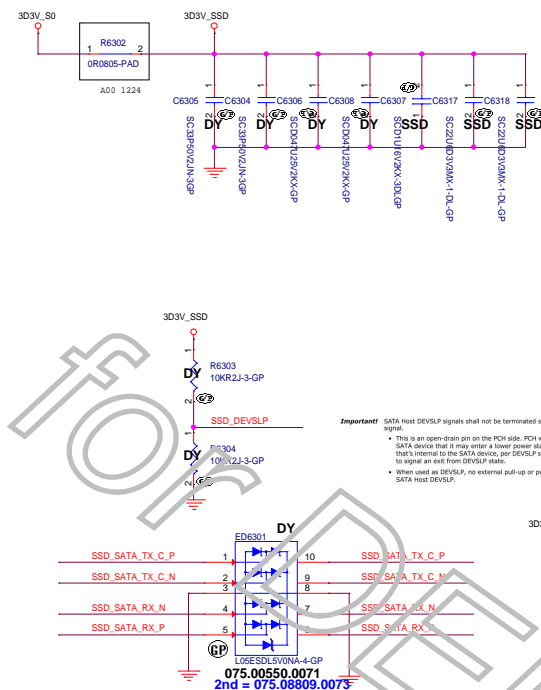
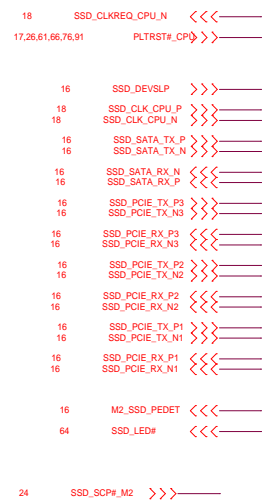


Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2 / SATA	PCI Express® Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

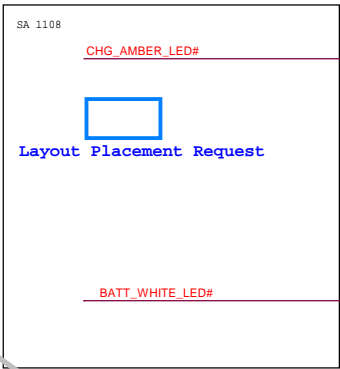
- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitor to support the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled QDS / devices are NOT used.
- Design Constraint: For PCIe® Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled QDS / Devices.**
- Design Constraint: For PCIe® Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled QDS / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Different Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe® lane that needs to support either **PCIe® Gen2 devices or PCIe® Gen3 devices**, follow the **PCIe® Gen 3/ SATA** multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled QDS / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

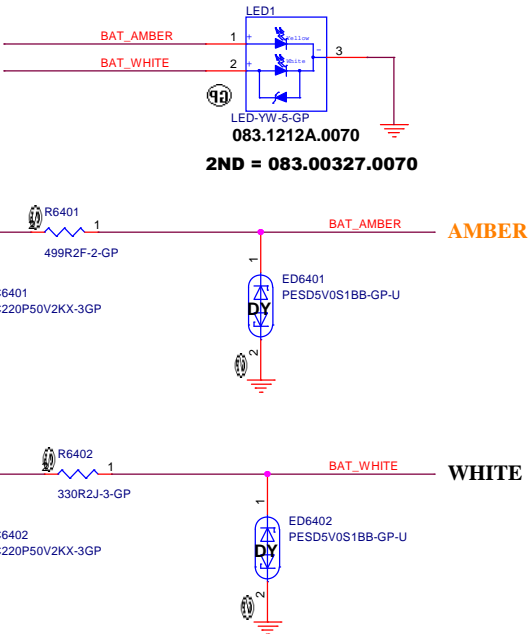
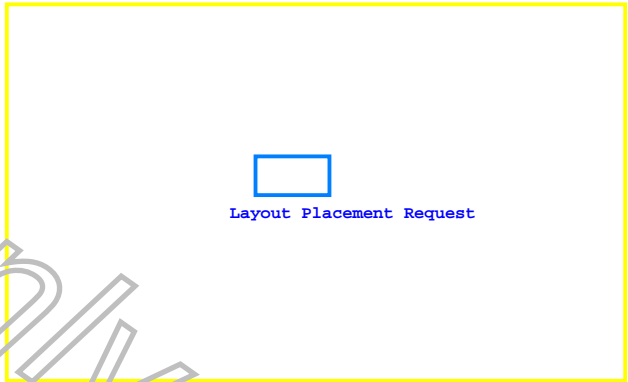
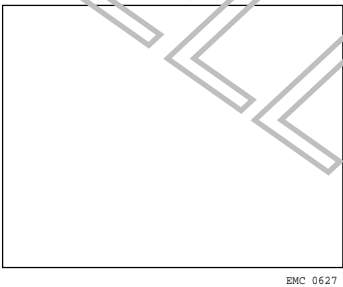
[illegible]Jedi UMA/DIS 2IN[®]

24,90 CHG_AMBER_LED# >>>—
24 BATT_WHITE_LED# >>>—

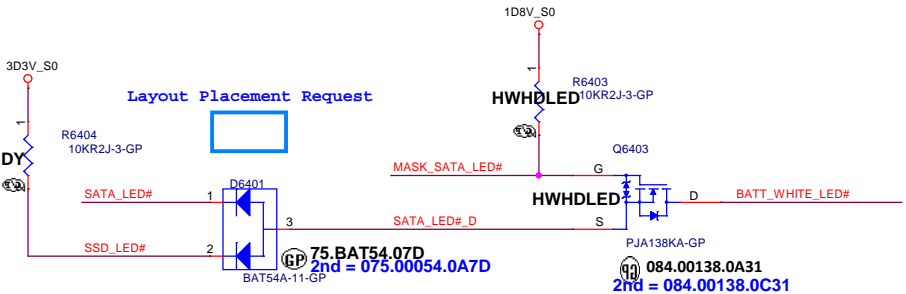
Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KPC GPIO



16 SATA_LED# >>>—
63 SSD_LED# >>>—
24 MASK_SATA_LED# >>>—

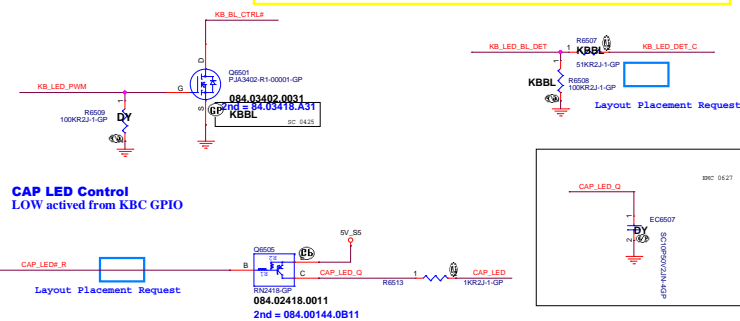
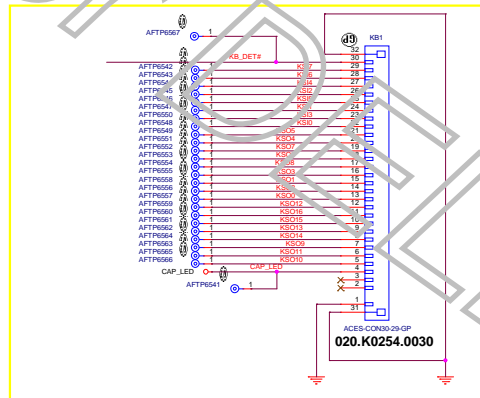
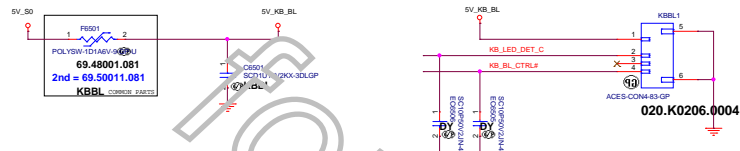
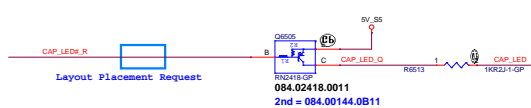


Main Func = Keyboard

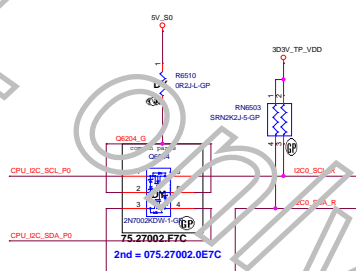
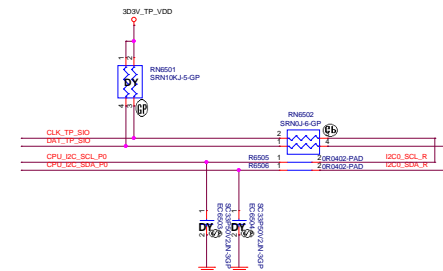
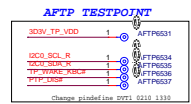
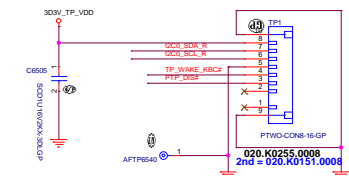
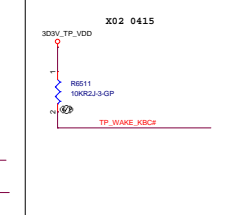
24 K50p.7] >>> _____
 24 K50p.16] <<< _____

24 PTP_DISA >>> _____
 3,24 TP_WAKE_KBC[<<< _____
 24 CLK_TP_SIO <<< _____
 24 DAT_TP_SIO <<< _____
 20,66 CPU_DC_SCL_P0 >>> _____
 20,66 CPU_DC_SDA_P0 >>> _____
 19 KB_LED_BL_DET <<< _____
 20 KB_LED_DET <<< _____
 24 KB_LED_PWM >>> _____
 24 CAP_LED_R >>> _____

KB Backlight Power Consumption: 285mA max.

CAP LED Control
LOW active from KBC GPIO

Main Func = TPAD

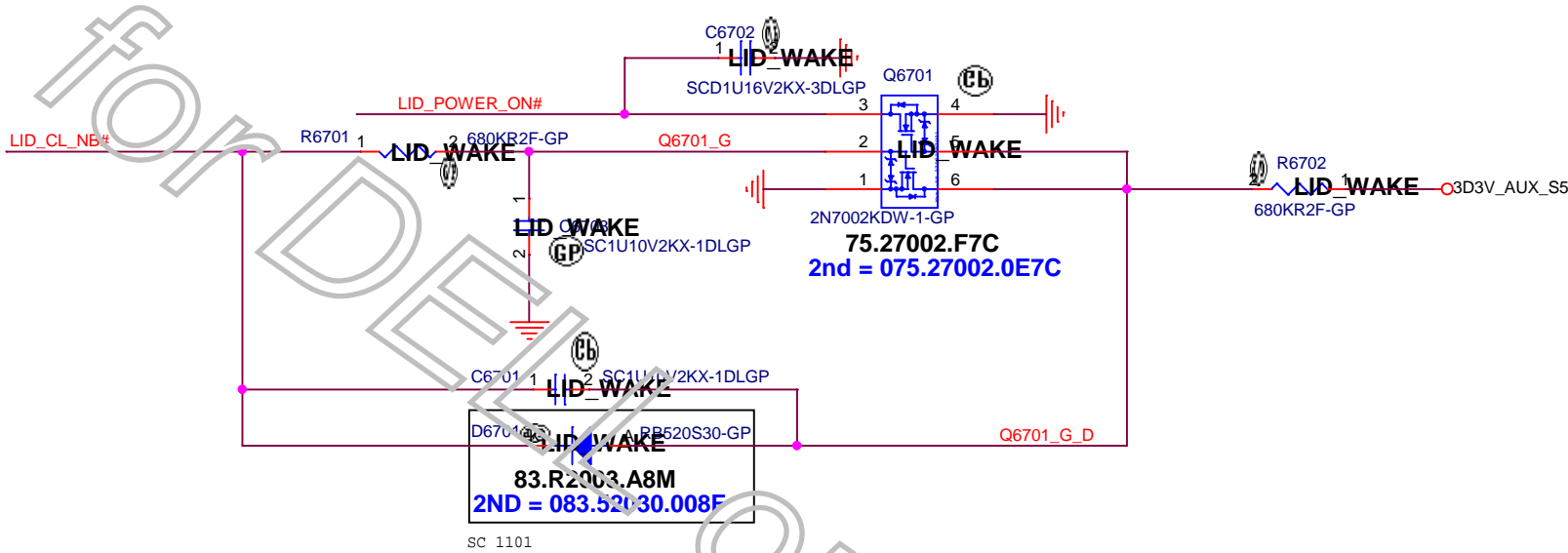
EC I2C
CPU I2CNeed to check if it is Active High or Active Low
and check if there is a pull-up on TPAD side.

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(P2)
8	CLK(P2)

Jed LMA/CHS 28/1

Main Func = HALL SENSOR

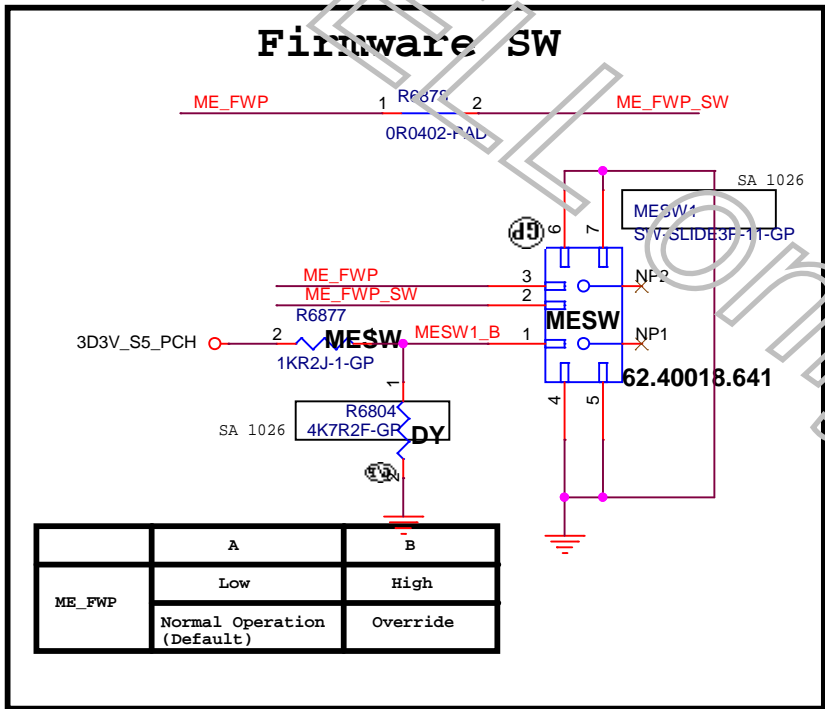
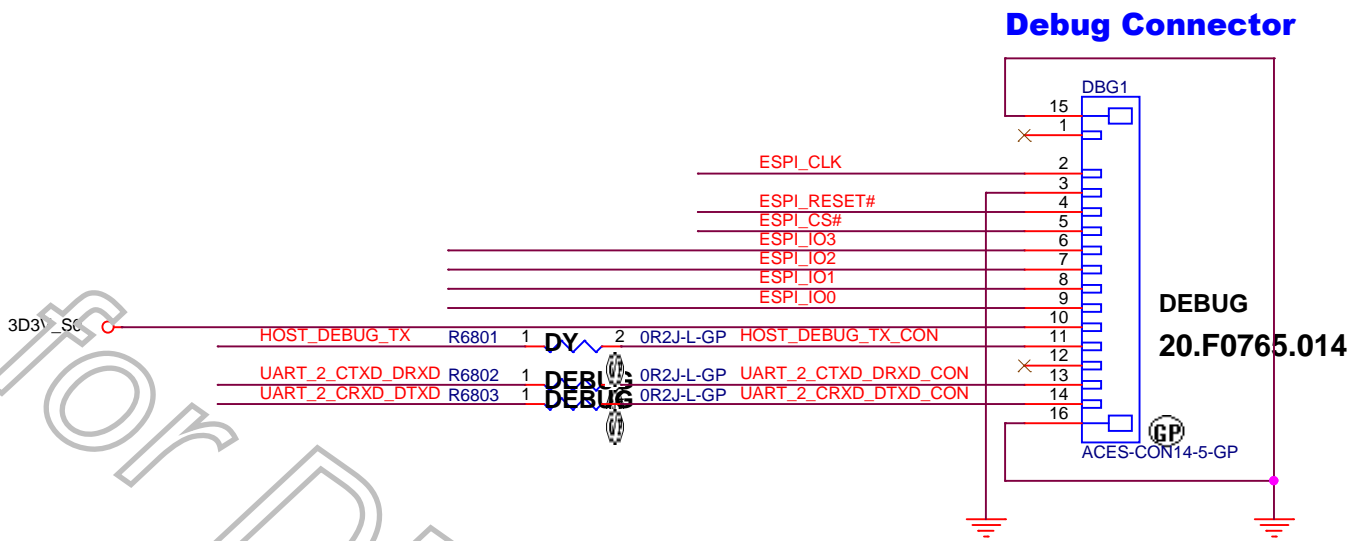
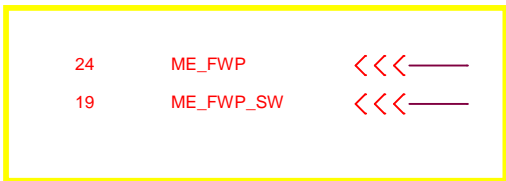
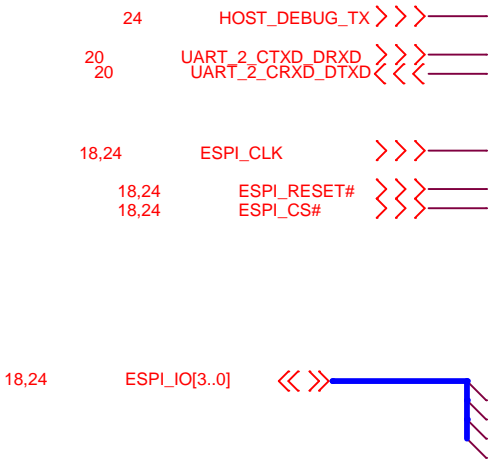
69 LID_CL_NB# >>>
LID_POWER_ON# <<<



<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Lid Wake					
Size A4	Document Number Jedi15"/17" WHL-U				Rev A00
Date: Tuesday, January 08, 2019			Sheet 67 of 106		

Main Func = Debug



Jedi UMA/DIS 2IN1

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Debug (LPC debug)**

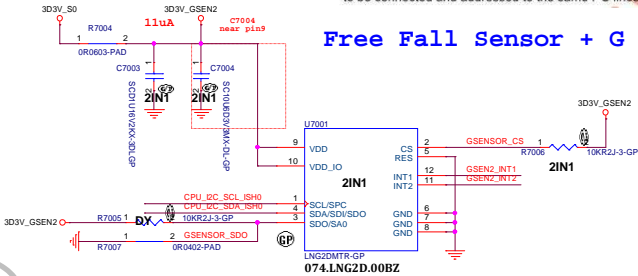
Size A4	Document Number Jedi15"/17" WHL-U	Rev A00
Date: Tuesday, January 08, 2019		Sheet 68 of 106

Main Func = Free Fall Sensor

20.55	CPU_DC_SCL_ISH0	<<>
20.55	CPU_DC_SDA_ISH0	<<>
20	GSEN2_INT1	<<<
18	FFS_INT1	<<<
20	FFS_INT2	<<<
60	FFS_INT2_Q	<<<

The slave address (SAD) associated to the LNG2DM is 010100xb. The SDO/SA0 pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor

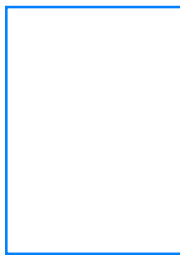


Layout Placement Request

Layout Placement Request

combine G

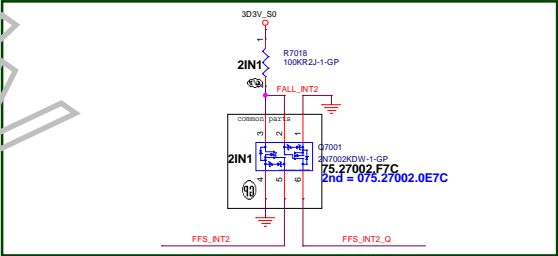
Layout Placement Request



Note:

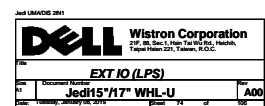
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U7001



Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.



for DELL only

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

EXT IO (TYPEC Redriver/MUX)

Size
A

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 75 of 106

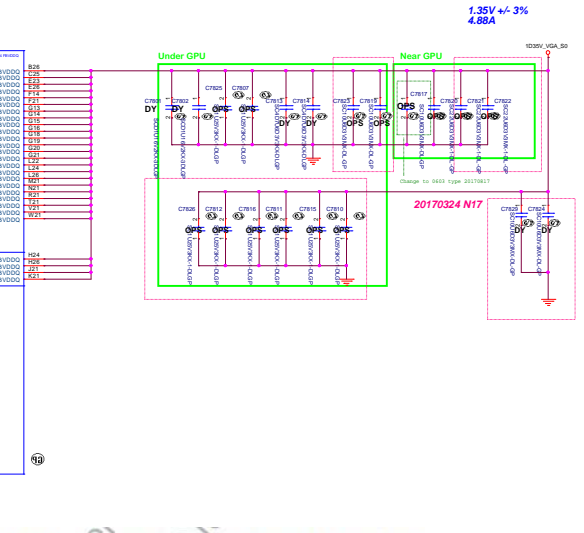
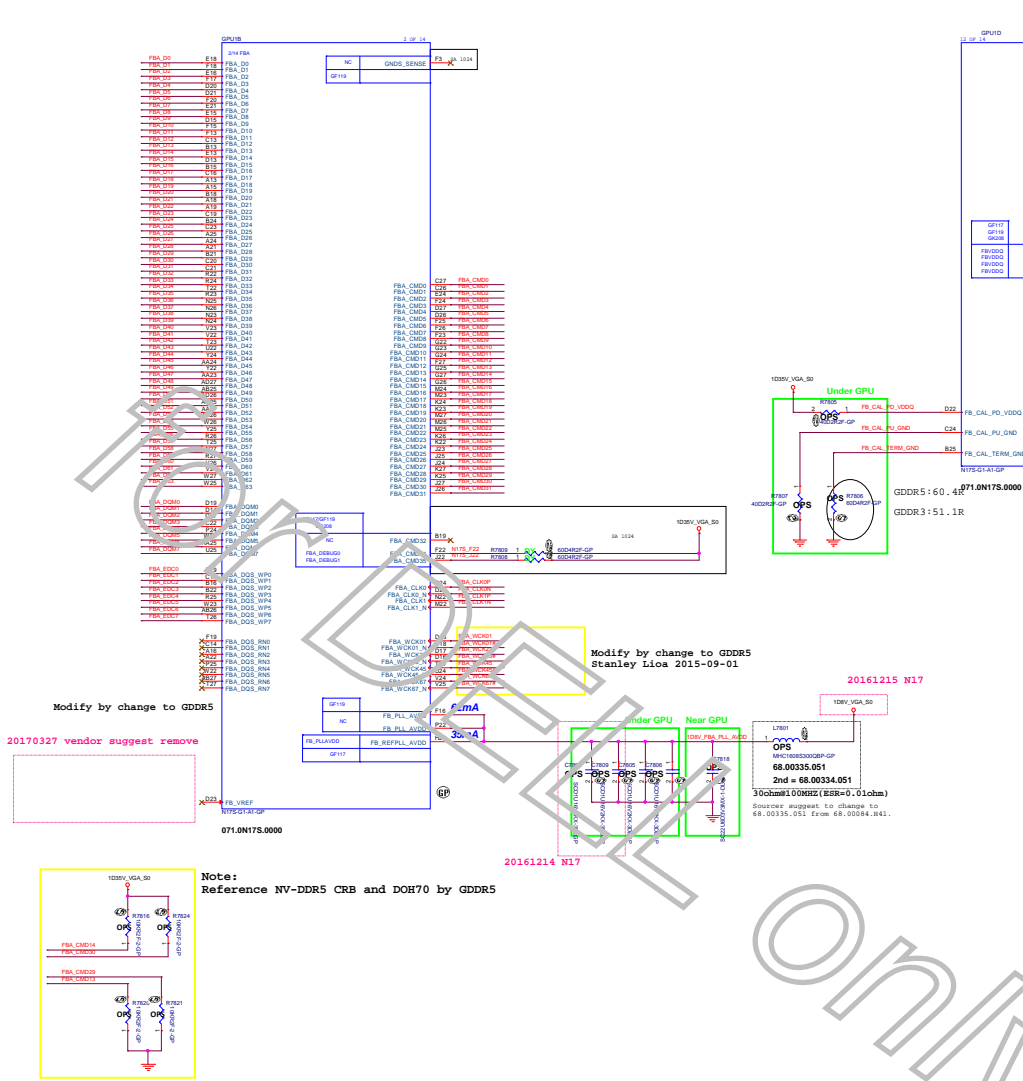
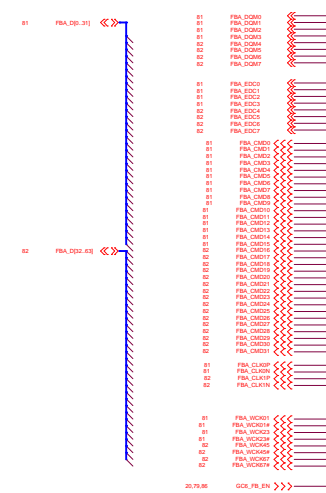


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FBVDD/IQ Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 μF	X7R	0402	2	0	Under GPU
	1 μF	X7R	0603	2	8	Under GPU
	4.7 μF	X6S	0603	2	0	Under GPU
	10 μF	X6S	0603	0	2	Under GPU
	10 μF	X6S	0603	1	1	Near GPU
	22 μF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FB PLL Supply Rail for GDDR5						
GB2B-64,	0.1 μF	X7R	0402	2	4	Under GPU
GB2C-64	22 μF	X6S	0805	1	1	Near GPU
Bead Type						
	30 Ω		0603	1	1	Near GPU
(ESR=0.010 Ω)						

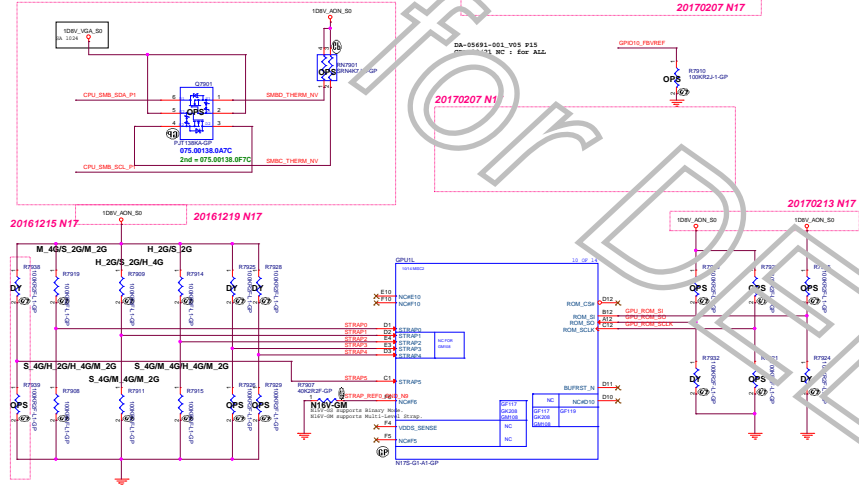
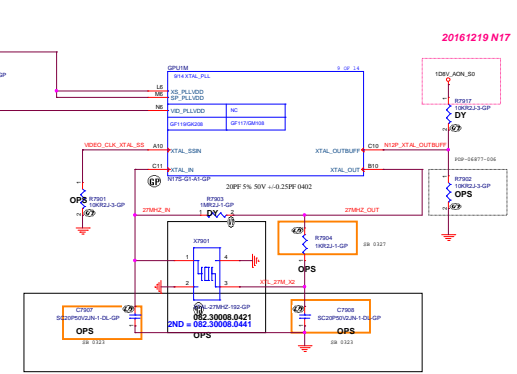
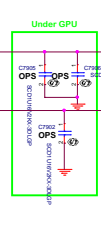
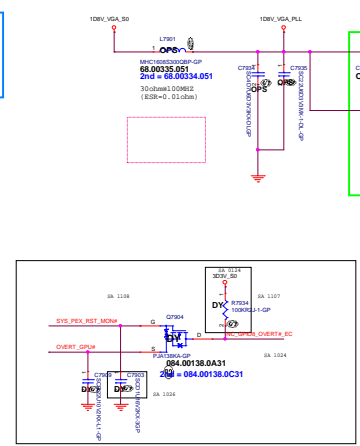
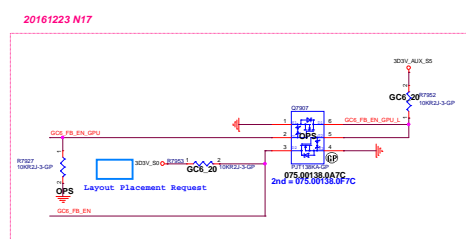


Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

00101010 M17

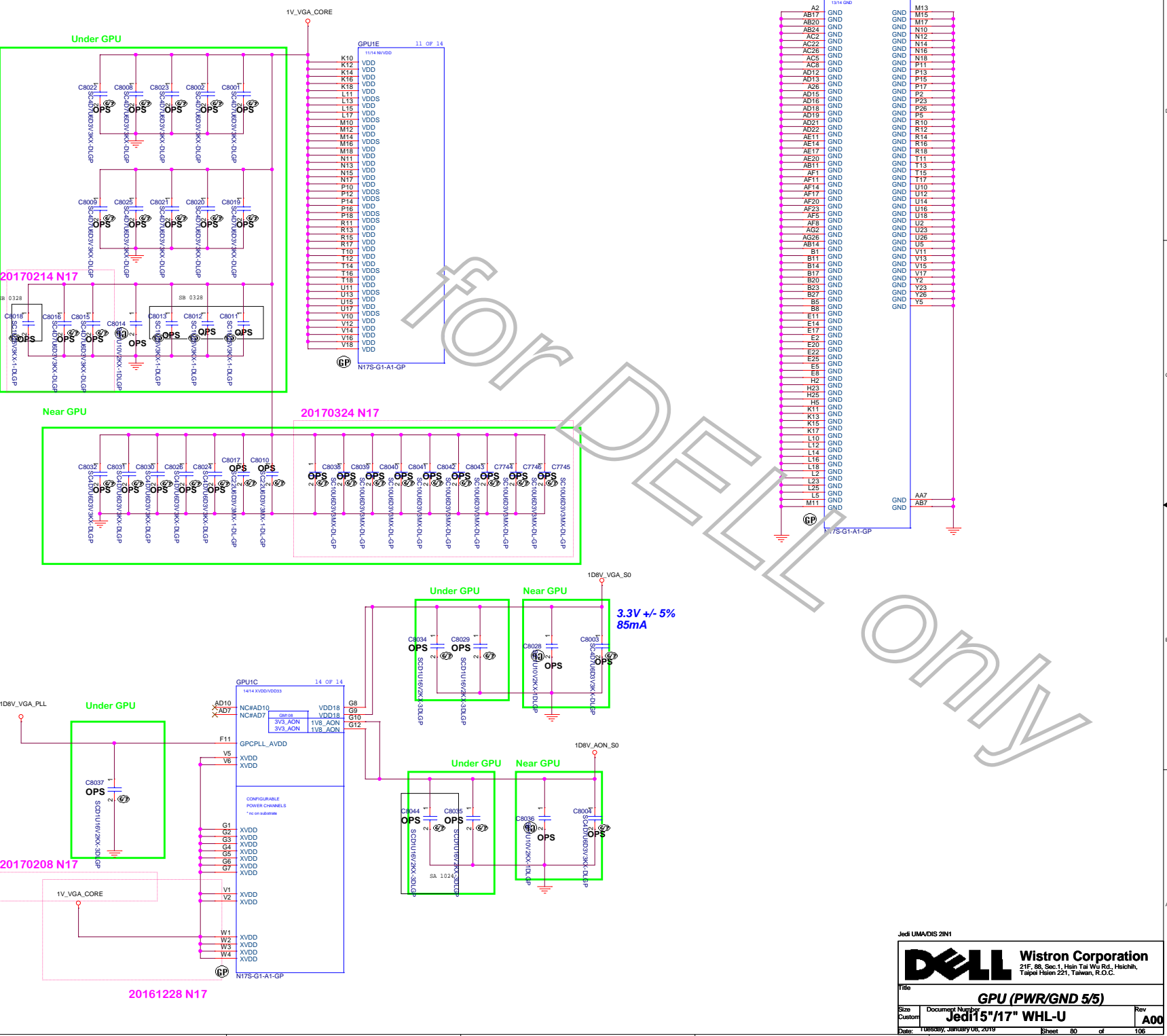


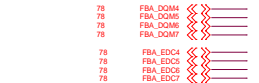
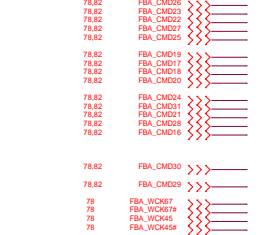
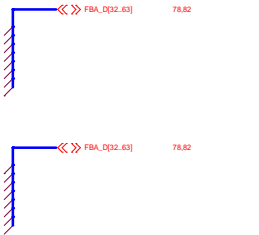
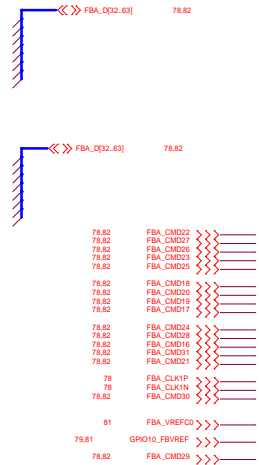
Row Index	Strap Pins				Resulting SORA_EXPOSED Enablements			
	SORA_S0	SORA_S1	SORA_S2	SORA_S3	SORA_0_EXPOSED	SORA_1_EXPOSED	SORA_2_EXPOSED	SORA_3_EXPOSED
15	L	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	L	H	H	ENABLED	disabled	disabled	disabled
11	L	H	L	L	ENABLED	disabled	disabled	disabled
10	L	H	L	H	ENABLED	disabled	disabled	disabled
9	L	H	H	L	ENABLED	disabled	disabled	disabled
8	L	H	H	H	disabled	disabled	disabled	disabled
7	M	X	X	X	(Reserved; do not configure)			
6	All other Strap Configurations				(Reserved)			

Strap Pins <small>(see Note)</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000) Samsung 2G
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004) Micron 2G
H	L	H	5 (0x0005) Hynix 2G
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
	M	L	9 (0x0009)
	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Memory Density	Allowed Memory Configuration	FBD/QDQ	Vendor	Manufacturer Part No.	Die Revision	Temp. Grade	Date Code	Qual. Pk.	Qual. Pk.	Grade	
8 Gb	256Kx12 512Kx10	1.35V	SamSung	K4G621238F-HC18	B-0e	Qw	0	0	N/A	Full	Substitution allowed with water
			SamSung	K4G621238F-HC18	B-0e	Qw	0	0	N/A	Full	Substitution allowed with water
			Microton	MT151256K2HIF-702-A	A-0e	Qw	1	0	N/A	Full	Substitution allowed with water
			Microton	MT151256K2HIF-80-A	A-0e	Qw	1	0	N/A	Full	Substitution allowed with water
			Hylix	H5G8C40160-RJC	A-0e	Qw	2	0	N/A	Full	Production ready
			Hylix	H5G8C40160-RJC	A-0e	Qw	2	0	N/A	Full	Substitution allowed with water
			Microton	MT151256K2HIF-702-B	B-0e	Qw	1	0	N/A	Full	Production ready
			Microton	MT151256K2HIF-80-B	B-0e	Qw	1	0	N/A	Full	Substitution allowed with water
			Hylix	H5G8C40160-RJC	A-0e	Qw	3	0	N/A	Full	Production ready
			Hylix	H5G8C40160-RJC	A-0e	Qw	3	0	N/A	Full	Substitution allowed with water
			Hylix	H5G8C40160-RJC	A-0e	Qw	5	0	N/A	Full	Production ready
			Hylix	H5G8C40160-RJC	A-0e	Qw	5	0	N/A	Full	Substitution allowed with water
4 Gb	128Kx12 256Kx16	1.35V	Hylix	H5Q4C40160-RJC	A-0e	Dw	8	0	N/A	Substitution allowed with water	

Main Func = dGPU



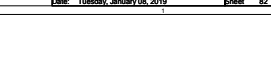
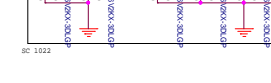
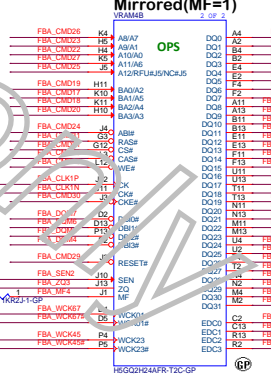
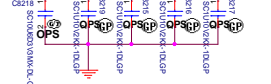
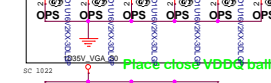
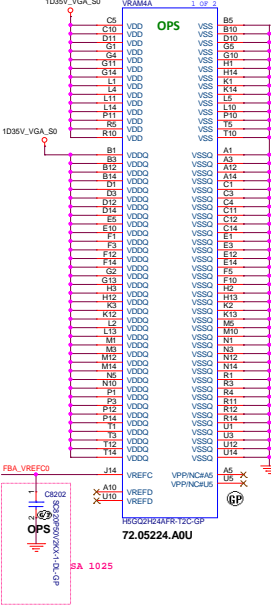


Frame Buffer Partition A-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (VRAM5,6 3/4)

Size
A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

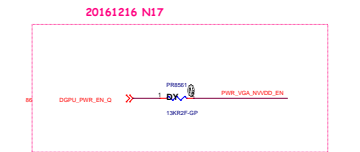
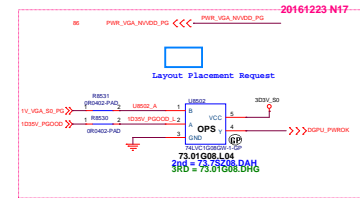
Sheet 83 of 106

for DELL only

Jedi UMA/DIS 2IN1

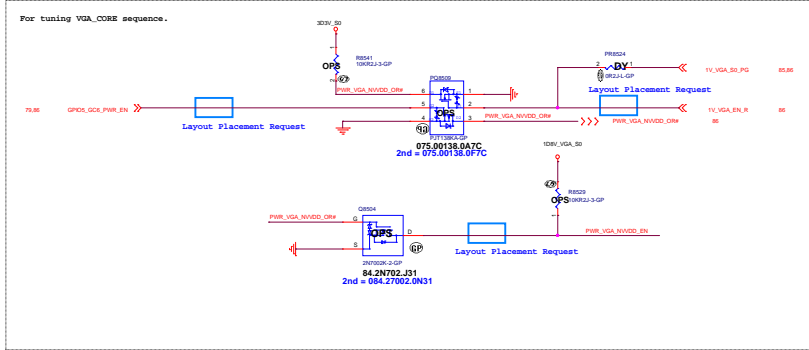
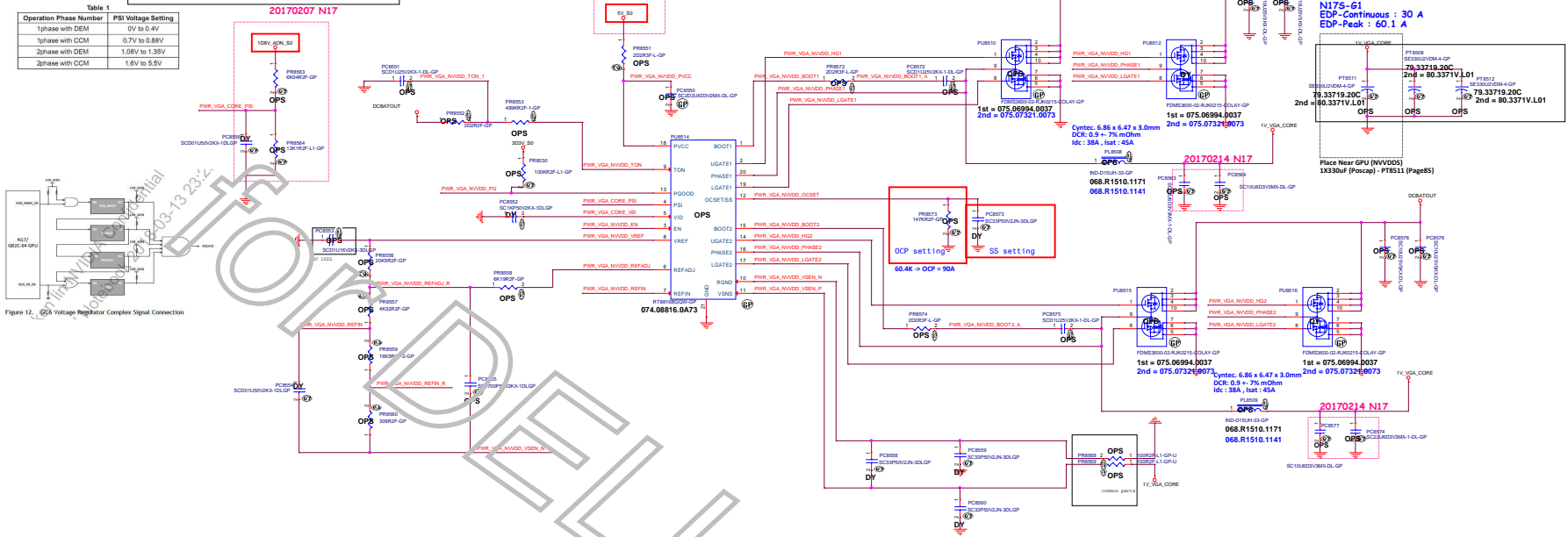
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU (VRAM7,8 4/4)			
Size A3	Document Number Jedi15"/17" WHL-U		Rev A00
Date: Tuesday, January 08, 2019		Sheet 84 of	106

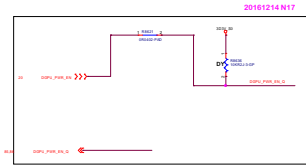
RT8816B For NVVDD



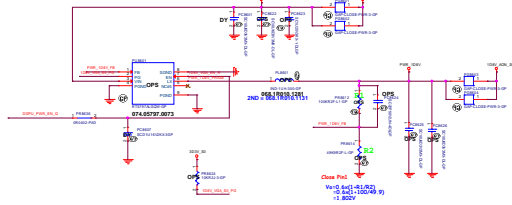
VGA : N17S-G1 / NVVDD
EDP-Continuous : 30A
EDP-Peak : 60.1A

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

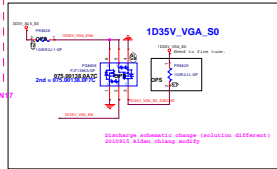
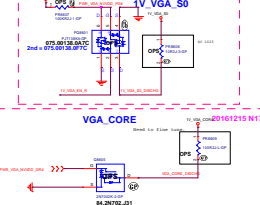




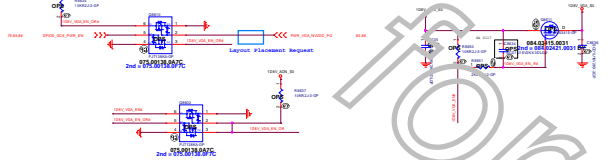
RT5707 for 1.8V_AON_S0



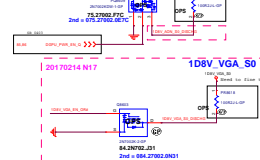
dGPU Power Discharge Circuit



1D8V_AON_S0 to 1D8V_VGA_S0



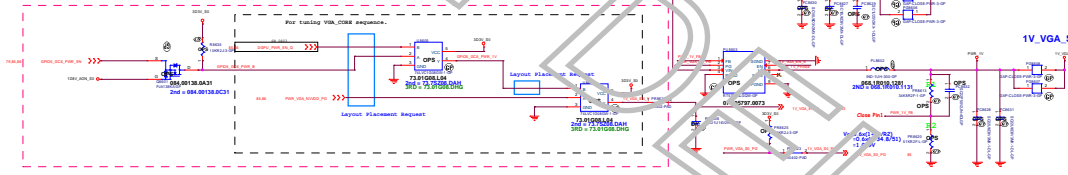
1D8V_AON_S0



1D8V_VGA_S0



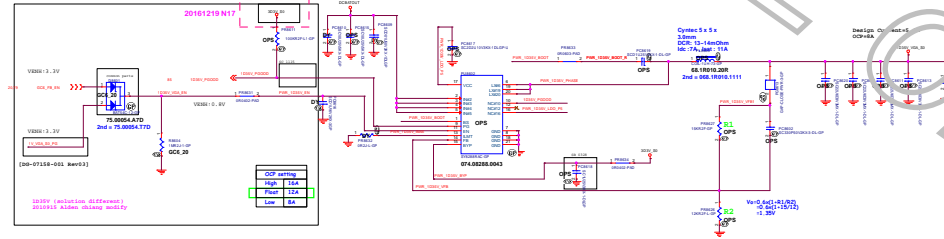
RT5797 for 1V_VGA_S0



1V_VGA_S0

1D35V_VGA_S0

SY2888RAC for 1D35V



for DELL only

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD)

Size
A3

Document Number

Jedi15"/17" WHL-U

Rev
A00

Date: Tuesday, January 08, 2019

Sheet 87 of 106

for DELL only

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

UNUSED PARTS (RSVD)

Size
A

Document Number

Jedi15"/17" WHL-U

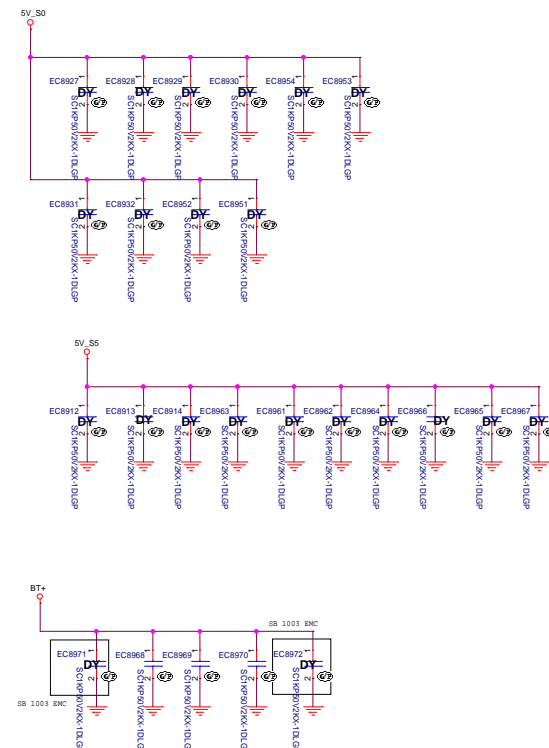
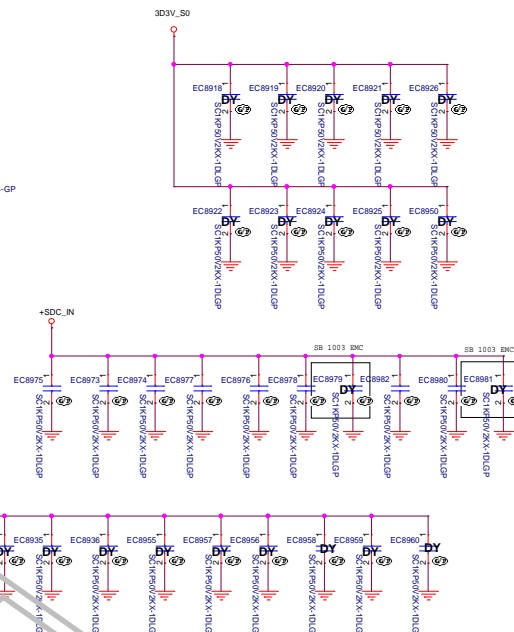
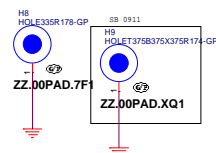
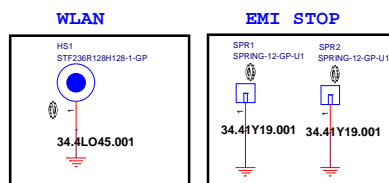
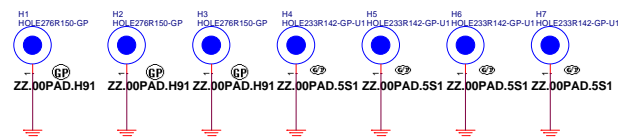
Rev

A00

Date: Tuesday, January 08, 2019

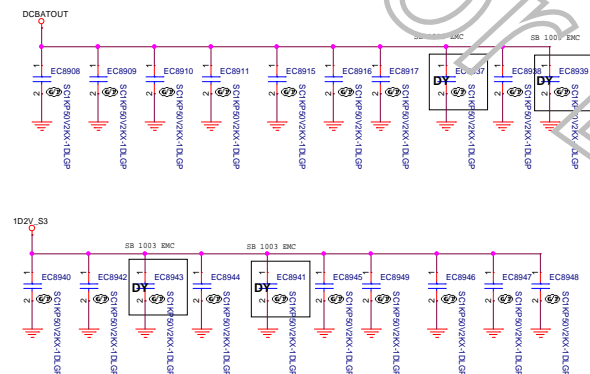
Sheet 88 of 106

Main Func = UnusedParts

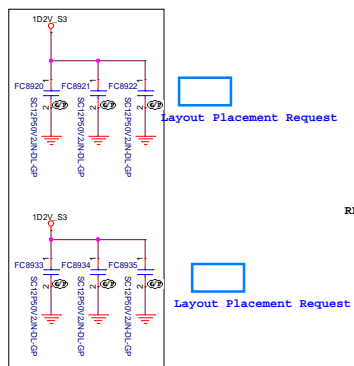


SSID = EMI

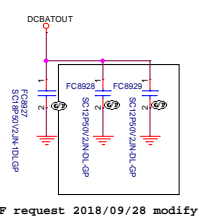
Mind the voltage rating of the caps.



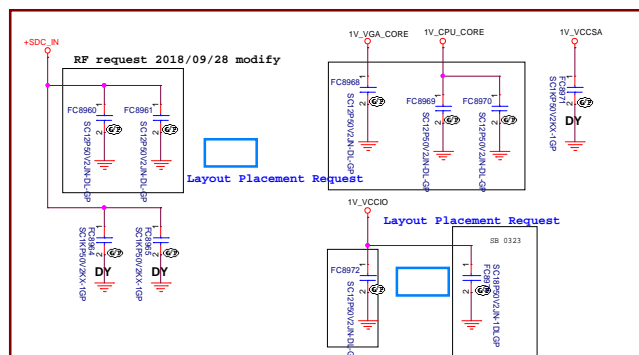
SSID = RF



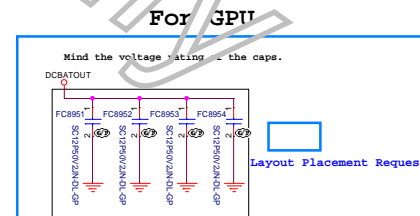
RF request 2018/09/28 modify



RF request 2018/09/28 modify

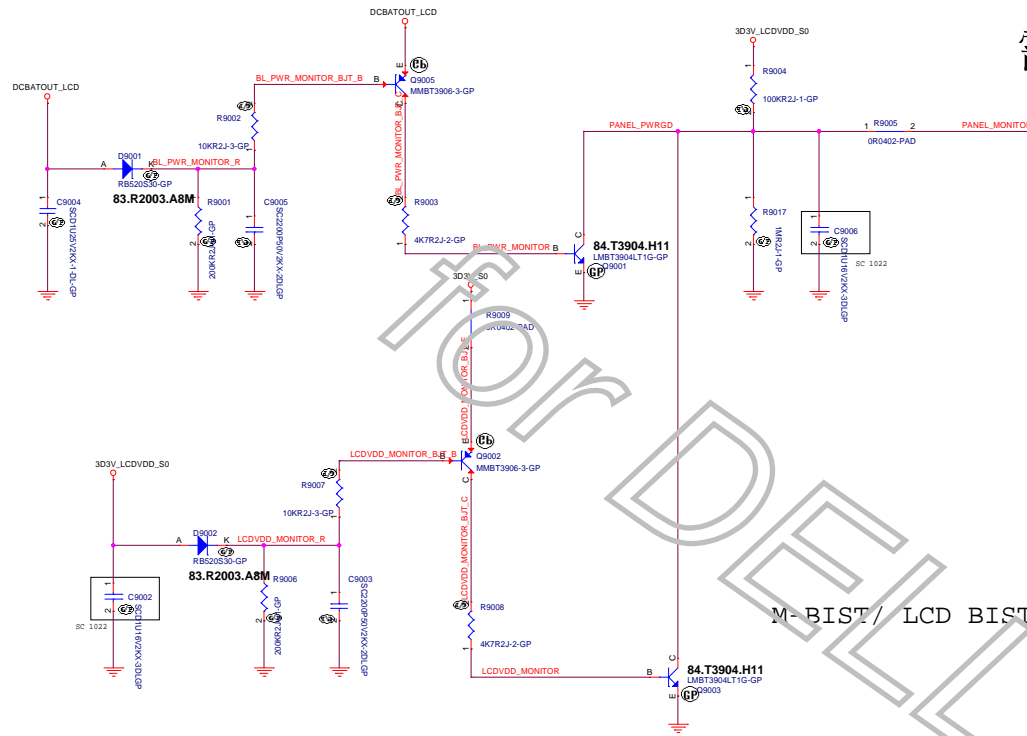


RF request 2018/09/28 modify

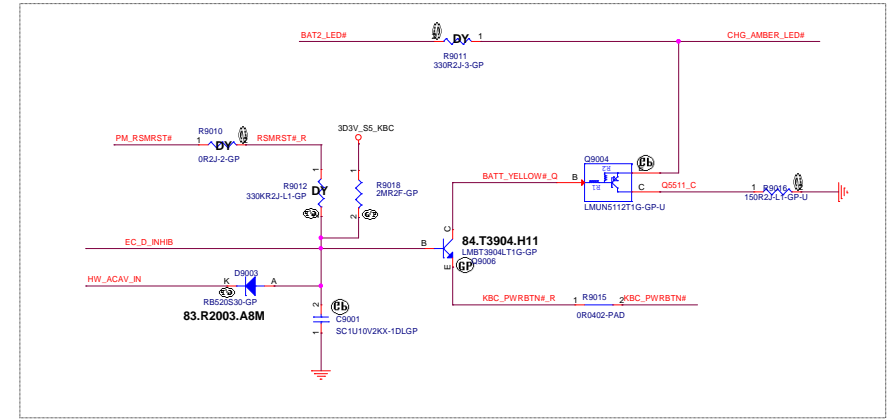


RF request 2018/09/28 modify

LCD BIST for G10 (Was test only for G9)



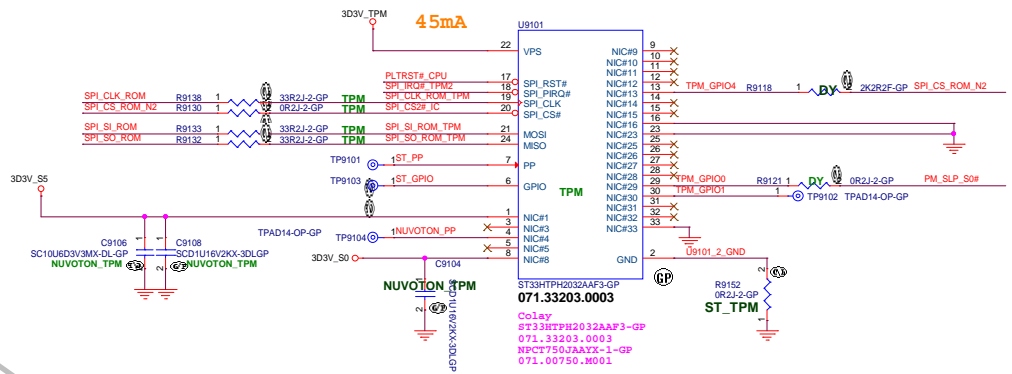
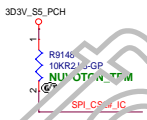
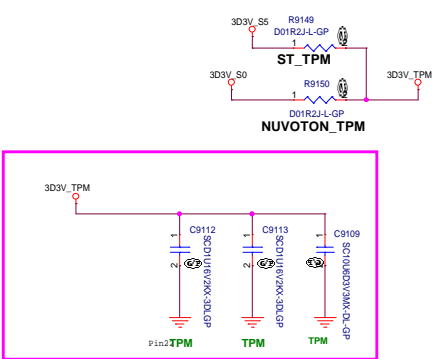
需確認 M-BIST for G10 (Proposed schematic)



M-BIST/ LCD BIST -1890201

Main Func = TPM

- 18,25 SPI_SO_ROM <<<
- 18,25 SPI_CLK_ROM >>>
- 15,18,25 SPI_SI_ROM >>>
- 18 SPI_CS_ROM_N2 <<<
- 17,26,61,63,66,76 PLTRST#_CPU >>>
- 17,24,40 PM_SLP_S0# >>>
- 20 PIRQ# <<<
- 18 TPM_SPI_IRQ# <<<



R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt_L (non TPM)	DY	DY

<Com Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Title **TPM2.0**

Size Custom Document Number **BOLT WHL** Rev **A00**

Date: Tuesday, January 08, 2019 Sheet 91 of 105

for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Finger Print

Size
A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 92 of 106

for DELL only

(Blanking)

Jedi UMA/DIS 2IN1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
A3	Jedi15"/17" WHL-U		A00
Date:	Tuesday, January 08, 2019	Sheet	93 of 106

for DELL only

(Blanking)

Jedi UMA/DIS 2IN1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A3	Document Number Jedi15"/17" WHL-U		Rev A00
Date: Tuesday, January 08, 2019		Sheet 94	of 106

for DELL only

(Blanking)

Jedi UMA/DIS 2IN1




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			(Reserved)	
Size	Document Number		Rev	
A3	Jedi15"/17" WHL-U		A00	
Date:	Tuesday, January 08, 2019	Sheet	95	of 106

for DELL only

(Blanking)

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size
A3

Document Number
Jedi15"/17" WHL-U

Rev
A00

Date: Tuesday, January 08, 2019

Sheet 96 of 106

for DELL only

(Blanking)

Jedi UMA/DIS 2IN1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS Switch

Size
A3

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 97 of 106

for DELL only

(Blanking)

Jedi UMA/DIS 2IN1



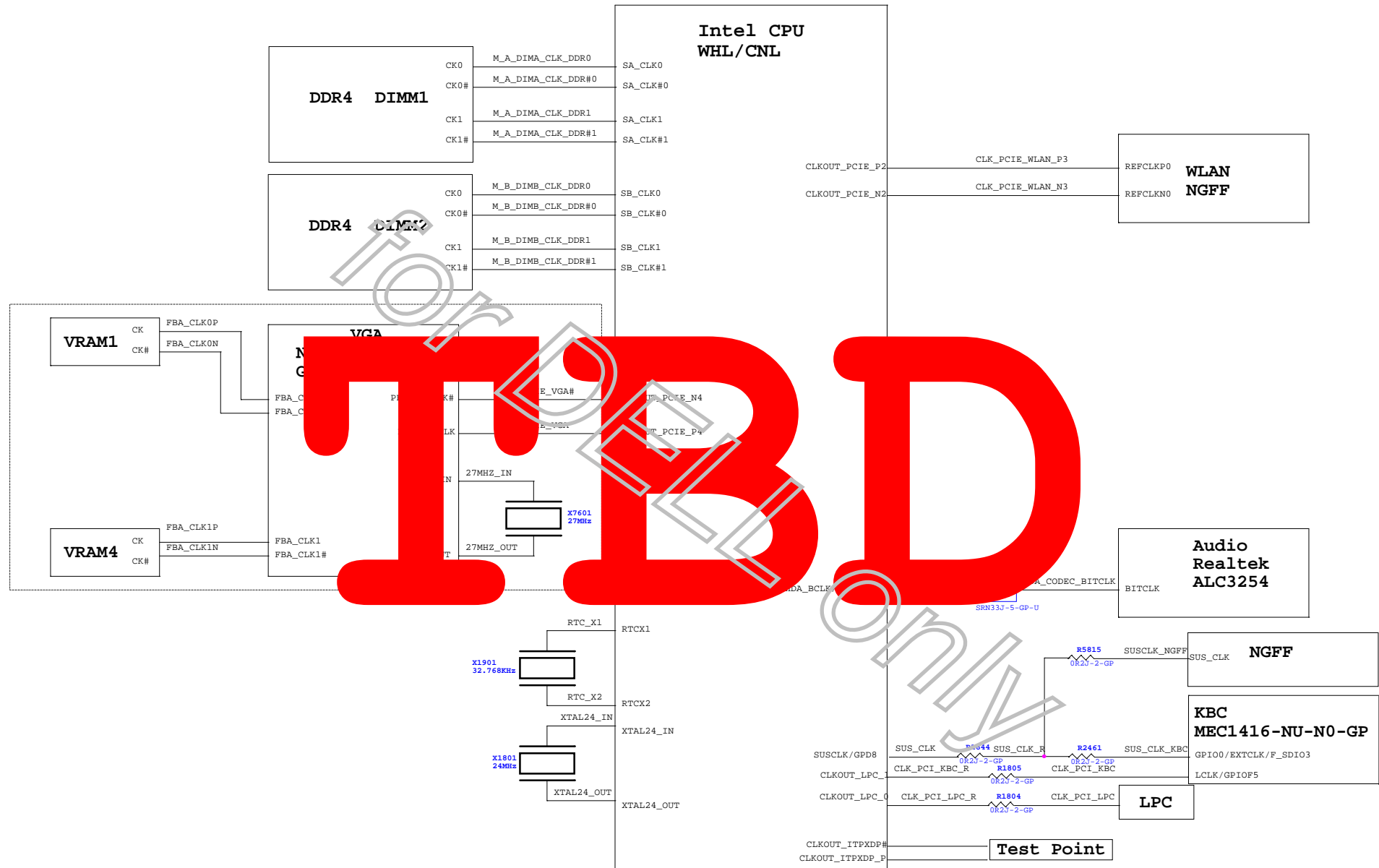
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CRT Switch		
Size	Document Number				Rev
A3	Jedi15"/17" WHL-U				A00
Date:	Tuesday, January 08, 2019		Sheet	98	of 106

Main Func = Debug (MIPI)

for DELL only

CLK Block Diagram

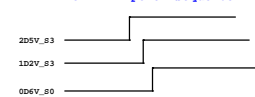


[illegible][illegible]

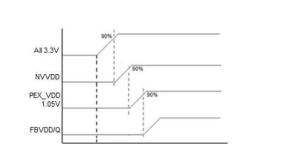
for DEFL only

		Wistron Corporation 21F, 88, Sec. 1, Hsien Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Change History			
Size A3	Document Number Jedi15"/17" WHL-U	Rev A00	
Date:	Tuesday, January 08, 2019	Sheet 101 of 106	

Timing diagram showing the relationship between 2D5V_S3, 1D2V_S3, and 0D6V_S0 signals. The signals are shown as digital waveforms. 2D5V_S3 is a high-frequency signal. 1D2V_S3 is a lower-frequency signal. 0D6V_S0 is a signal that transitions from low to high after 1D2V_S3 transitions from low to high.



[00-071588-001_v01]



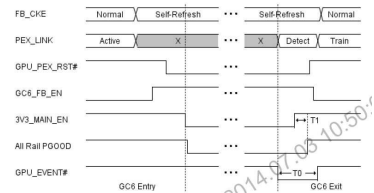
■

- The ramp time for any rail must be more than 40 ns and is less than 2ms

- Copyright © 2014 Wolters Kluwer Health | Lippincott Williams & Wilkins

There is no specific power down sequence. I

The following timing diagram in Figure 18.12 an

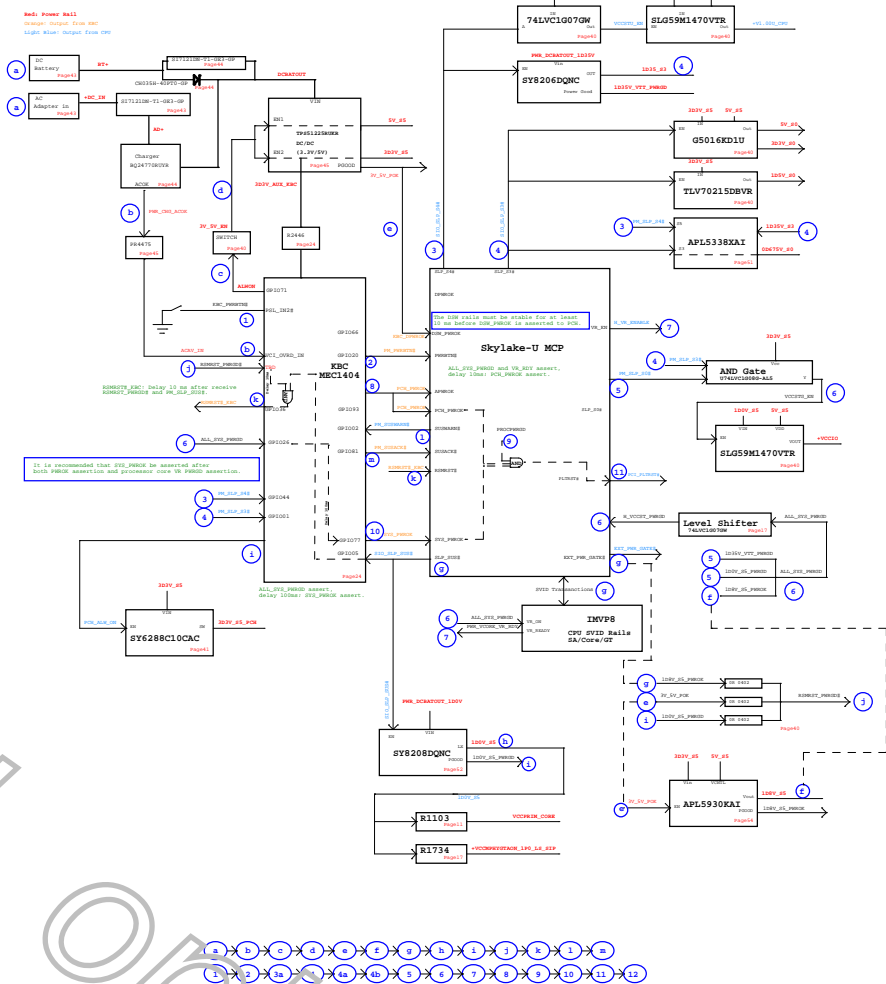


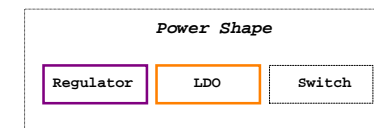
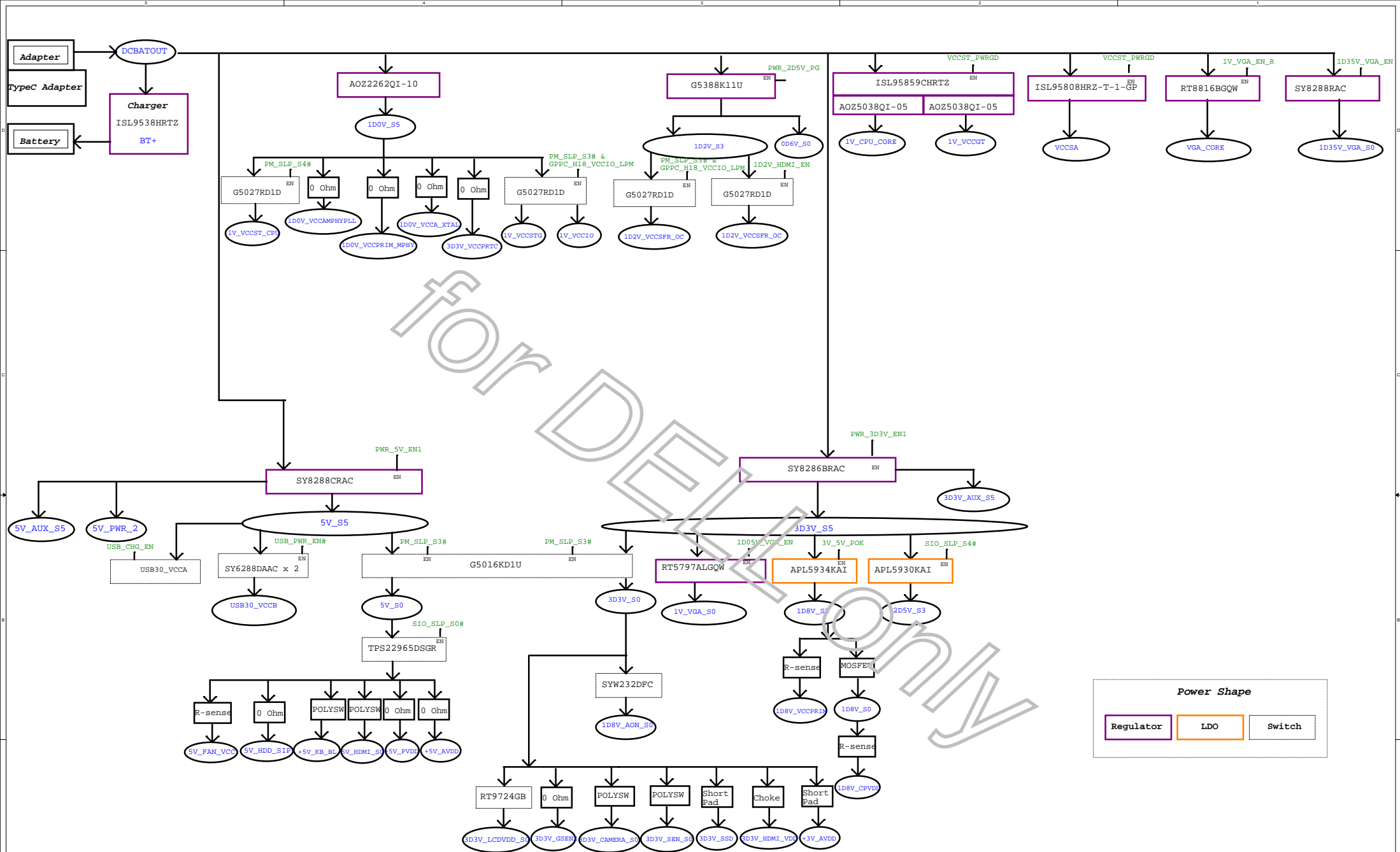
Symbol	Description	Min	Max
--------	-------------	-----	-----

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

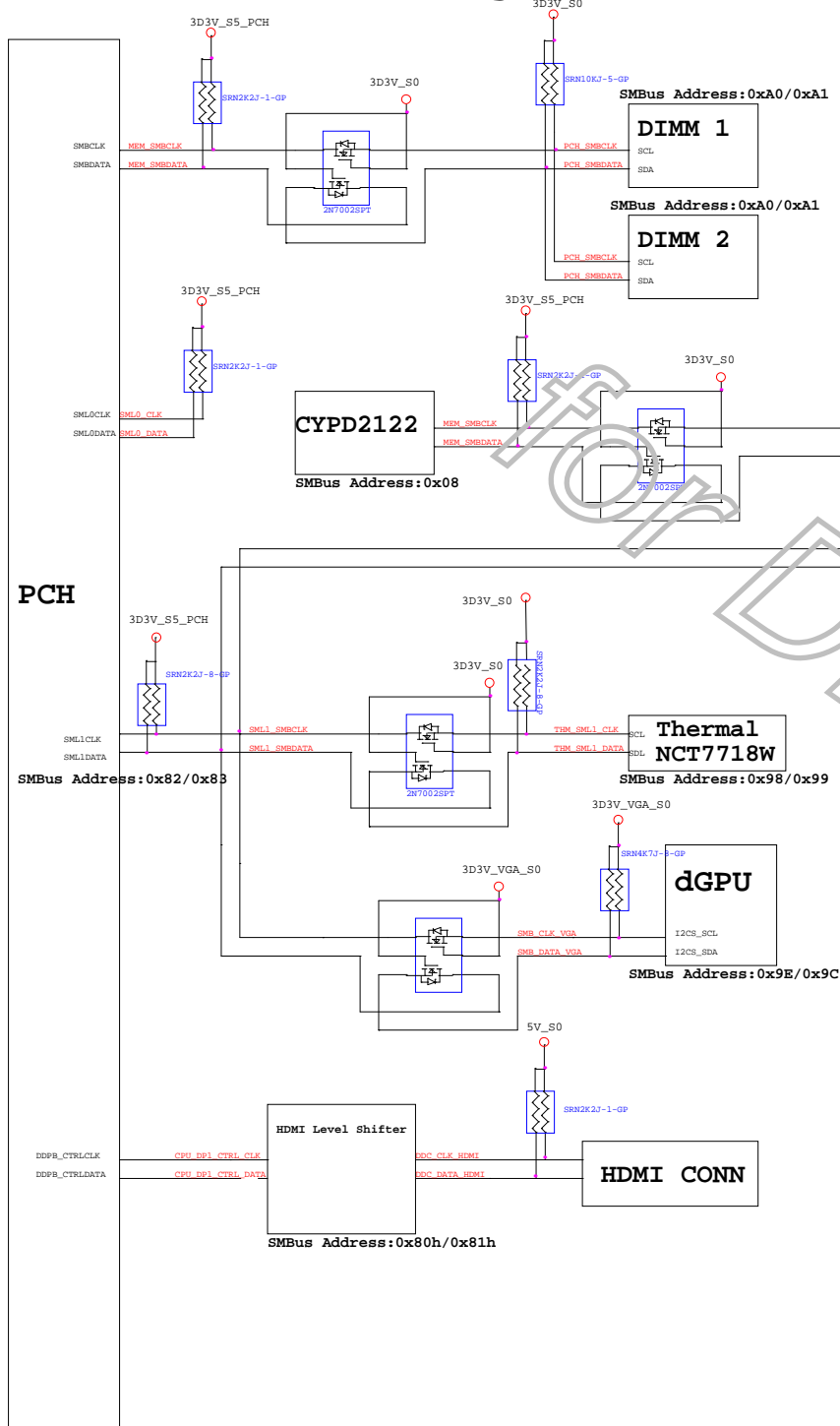
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation.

- any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

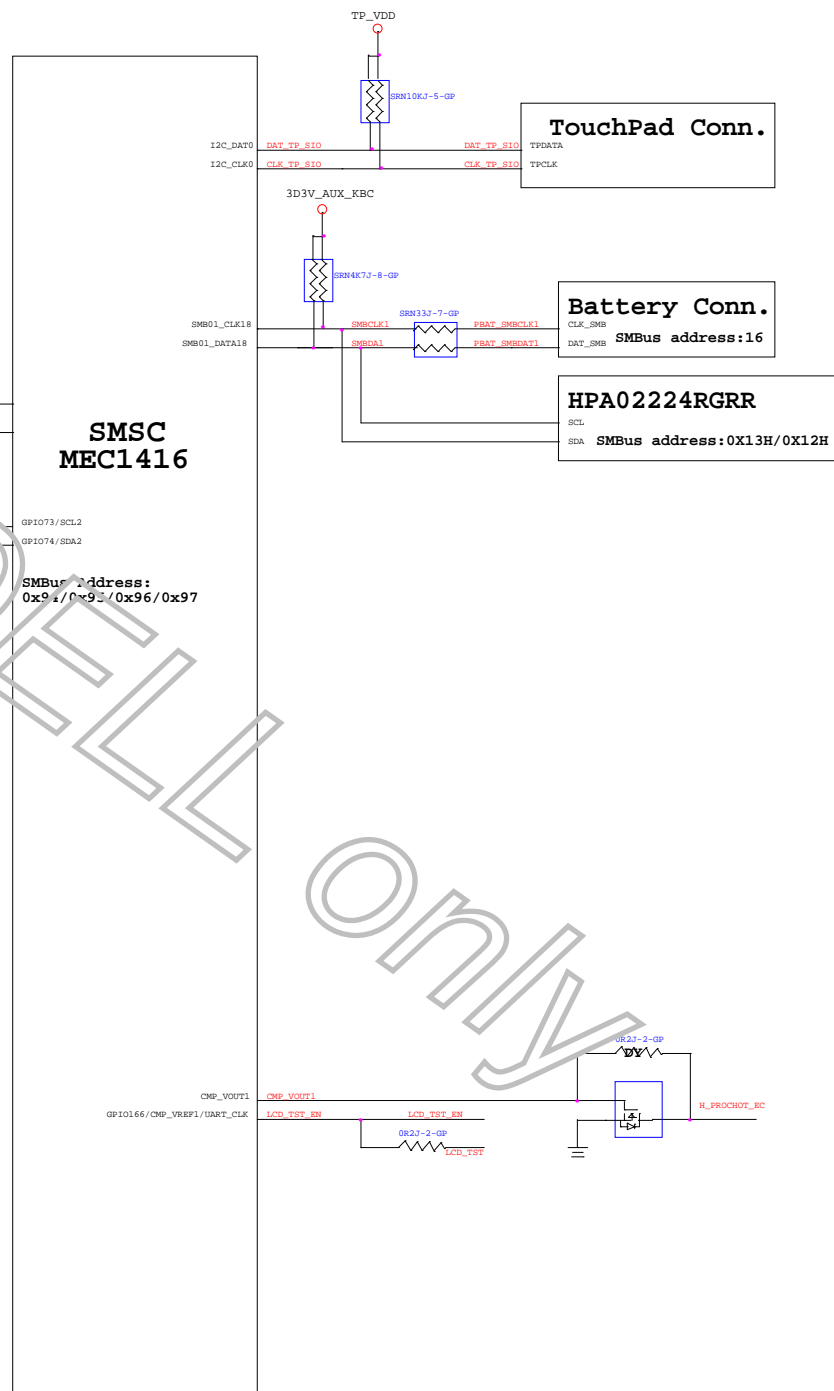




PCH SMBus Block Diagram

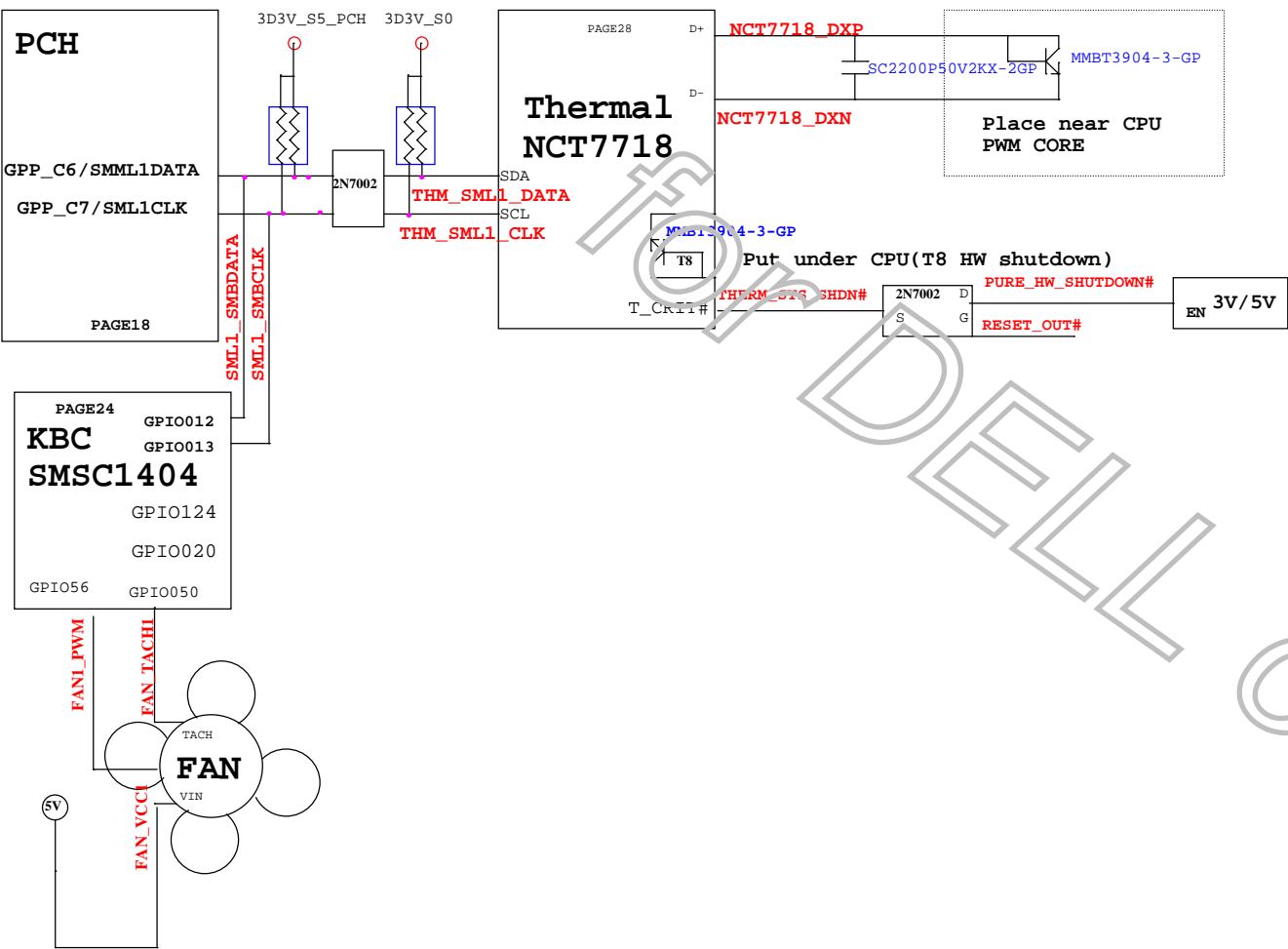


KBC SMBus Block Diagram

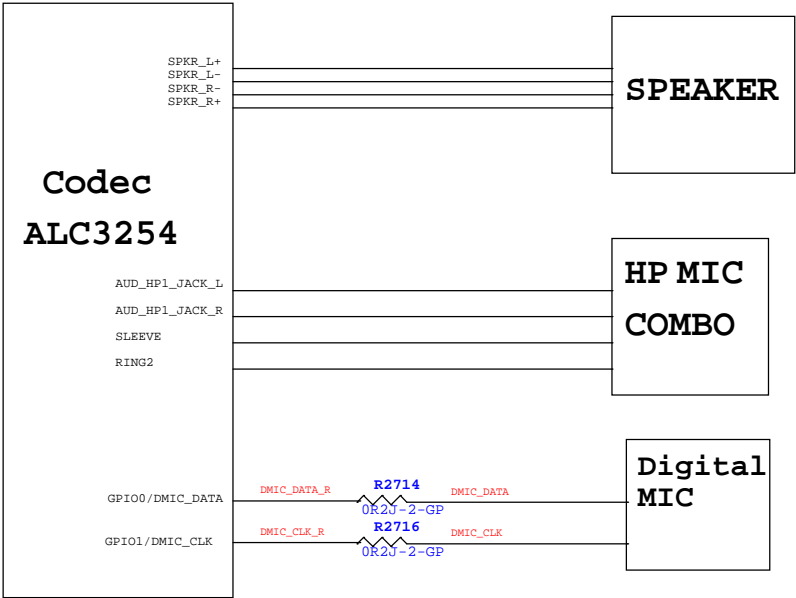


Jedi UMA0IS 2N1

Thermal Block Diagram



Audio Block Diagram



for DELL only

Jedi UMA/DIS 2IN1



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SIP connector

Size
A

Document Number

Jedi15"/17" WHL-U

Rev

A00

Date: Tuesday, January 08, 2019

Sheet 106 of 106